H61H2-TAIO Rev : B

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V.A	2011/07/19	Base on MRS H61H2-TAIO V:1.1
V.B	2011/10/12	Base on MRS H61H2-TAIO V:1.4
	2011/10/12	1. F_PANEL1 & F_ANEL2 Change Pin-define(inverse)
		2. Port D(DP) change to Port C(DP)
		3. PWM IC Change to NCP6153

Note:
design by
428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev2_0.pdf
443554_443554_Intel_6_Series_C200_Series_Chipset_EDS_rev2_1

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Title: Cover Page		
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PCB:229.9x190.3;6 layers

Signal
Power
Signal
Signal
Gnd
Signal

Sandy Bridge
Desktop Processor
Socket H2

MXM 3.0 — PCIE X16

DDR3 Channel A
DDR3 Channel B

SO-DIMM(DDR3)
1333MHz/1066MHz
Total Max 8GB

DVI

SCALER DP701

VGA in

DP

LVDS

Panel

FDI

DMI

H61
Cougar Point
Chipset

Wireless LAN — PCIe

TV Tuner — PCIe

SATA — SATA II BW:3.0G/s

RJ-45 CONN — Realtek RTL8111E_VL — PCIe

LPC

Super I/O IT8772

SPI ROM 32 M

HD AUDIO — ALC662_VD

Side I/O Line Out Mic In

Rear I/O Line Out

Audio Amplifie ALC113-GR

Speak R 5W

Speak L 5W

USB

Rear I/O USB 4Port

Side I/O USB 2 Poet

Web cam+MIC

RTS5139 Card reader

Touch screen

RF 2.4G

Panel Button

Power | VOL DOWN | VOL UP | Bright DOWN | Bright UP | Mode

SIDE IO

Card reade

USB

USB

Line_Out

Mic_In

Rear IO

DC-IN | LAN | Line Out | VGA IN | USB | USB | USB | USB

Feature Set	SKU Name					
	Q67	Q65	B65	H67	P67	H61
PCI Express* 2.0 Ports	8	8	8	8	8	6
PCI Interface	Yes	Yes	Yes	No	No	No
USB 2.0 Ports	14	14	12[6]	14	14	10[7]
SATA Ports (3.0 Gb/s & 1.5 Gb/s only)	4	5	5	4	4	4
SATA Ports (6.0 Gb/s & 3.0 Gb/s & 1.5 Gb/s)	2[4]	1[5]	1[5]	2[4]	2[4]	0[8]

4. SATA 6 Gb/s support on Port 0 and Port 1. SATA Ports also Support 1.5 Gb/s and 3.0 Gb/s.
5. SATA 6 Gb/s support on Port 0 only. SATA Port also Support 1.5 Gb/s and 3.0 Gb/s.
6. USB ports 6 and 7 are disable.
7. USB ports 6, 7, 12 and 13 are disabled
8. SATA Ports 2 and Ports 3 are disabled

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Title: Block Diagram

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PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO1	VCC3	DP701_ACK(SCALER)	GPI
GPIO2	VCC3	PCH_VOL_P	GPI
GPIO3	VCC3	PCH_VOL_N	GPI
GPIO4	VCC3	ALERT(MXM)	GPI
GPIO5	VCC3	OVERT(MXM)	GPI
GPIO6	VCC3	DP701_IRQ(SCALER)	GPI
GPIO7	VCC3	SPI_WP0_L(BIOS_WP)	GPI
GPIO9	3VSB	USB_OC_L5	Native
GPIO10	3VSB	USB_OC_L6	Native
GPIO13	3VSB	LPC_PME_L	GPI
GPIO14	3VSB	USB_OC_L7	Native
GPIO15	3VSB	TLS_EN	GPO
GPIO24	3VSB	PCH_SKTOCC_L	GPO
GPIO27	3VSB	LCD_SEL1	GPI
GPIO31	3VSB	LCD_SEL2	GPI
GPIO32	VCC3	WP_GPIO1	GPO
GPIO33	VCC3	WP_GPIO2	GPO
GPIO40	3VSB	USB_OC_L1	Native
GPIO41	3VSB	USB_OC_L2	Native
GPIO42	3VSB	USB_OC_L3	Native
GPIO43	3VSB	USB_OC_L4	Native
GPIO49	VCC3	WLAN_DIS	GPI
GPIO57	3VSB	LCD_SEL3	GPI
GPIO59	3VSB	USB_OC_L0	Native

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP22	3VSB	Power LED	
GP23	3VSB	Power LED	

PCH-INT Function

Function	INT Port	PCIE_X1 Port	Chipset
LAN Ethernet Controller	INT A#	PE_TX/RX_5	RTL8111E-VL
SATA Controller	INT B#	N/A	H61(COUGARPOINT)
Wireless	INT C#	PE_TX/RX_3	Mini PCIE

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Title: GPIO Function Map

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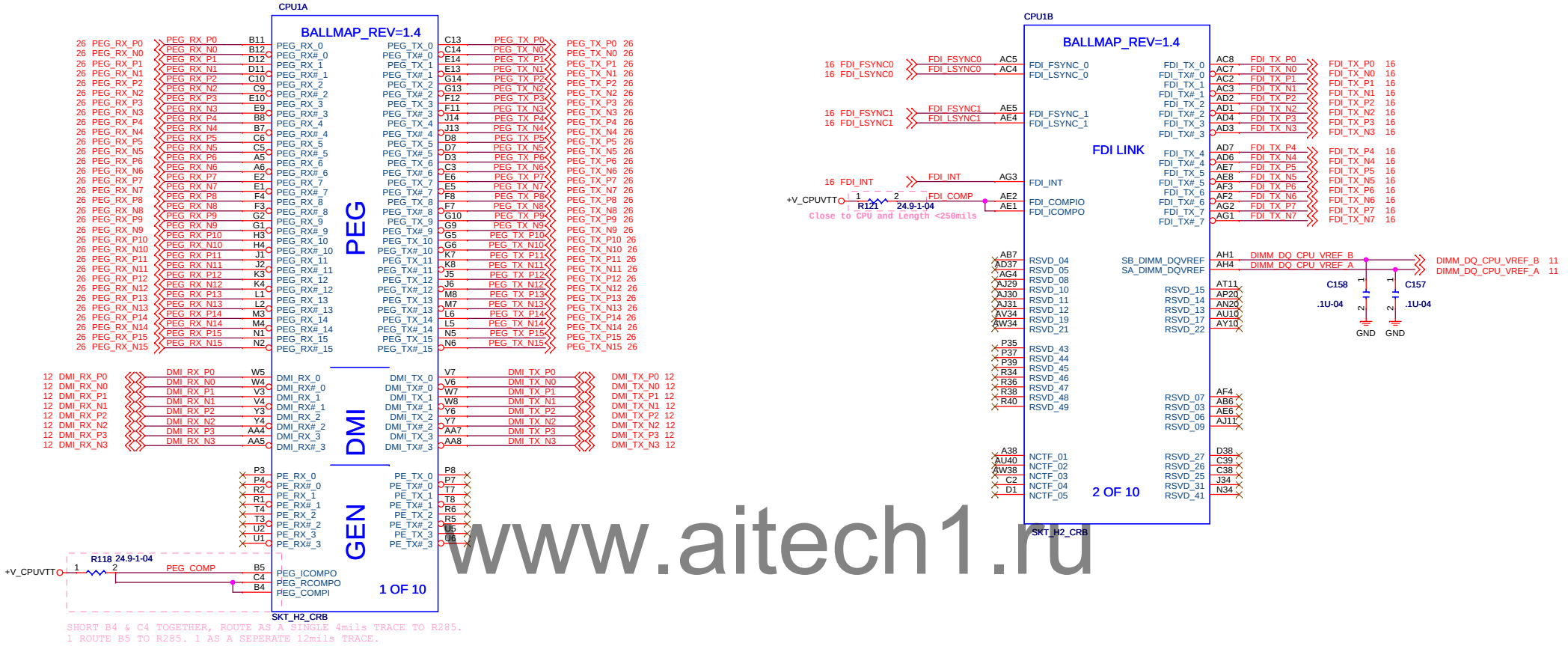

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Title	CPU - DMI/FDI/PEG		
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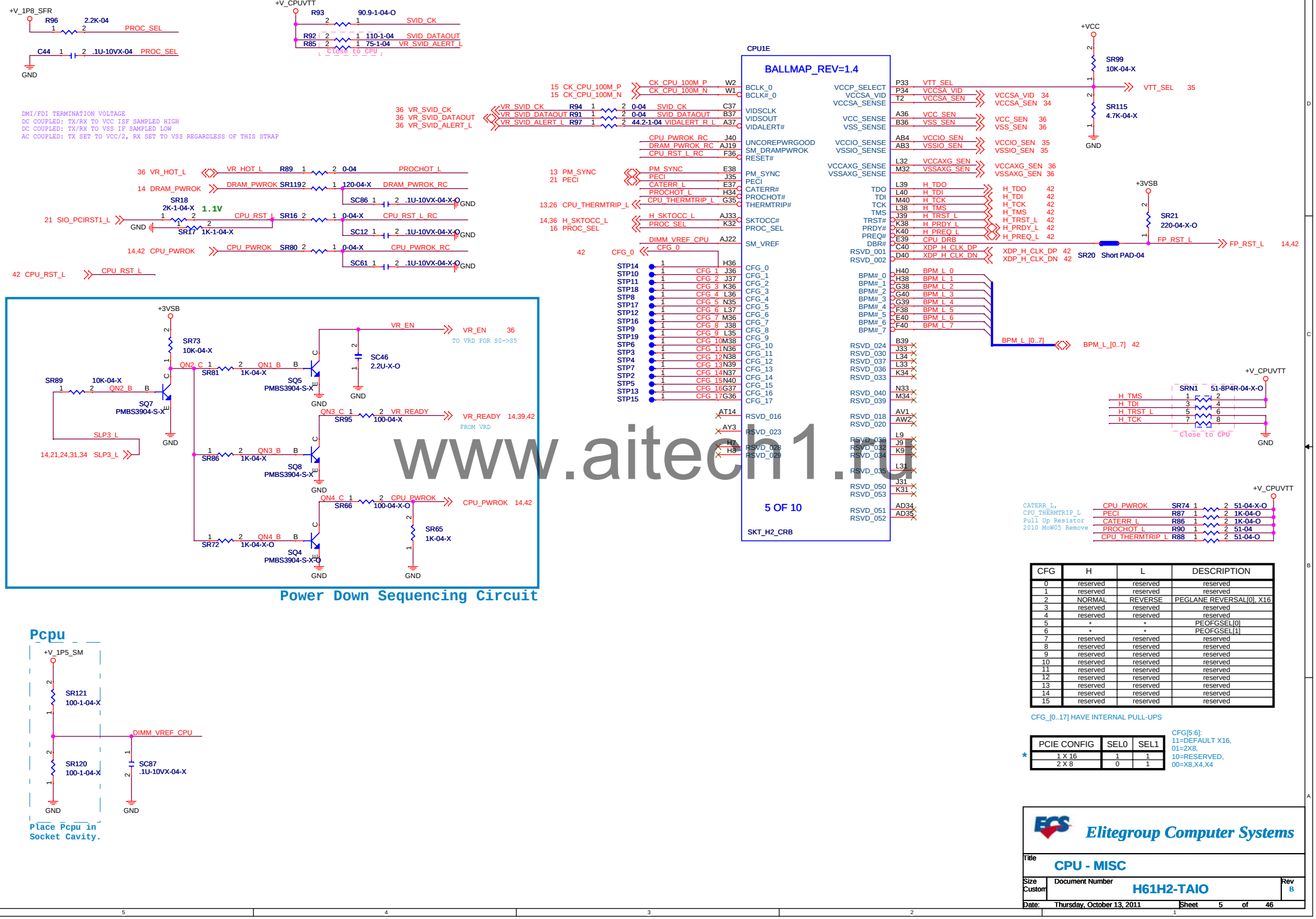

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

*	PCIE CONFIG	SEL0	SEL1
	1 X 16	1	1
	2 X 8	0	1

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Title: CPU - MISC

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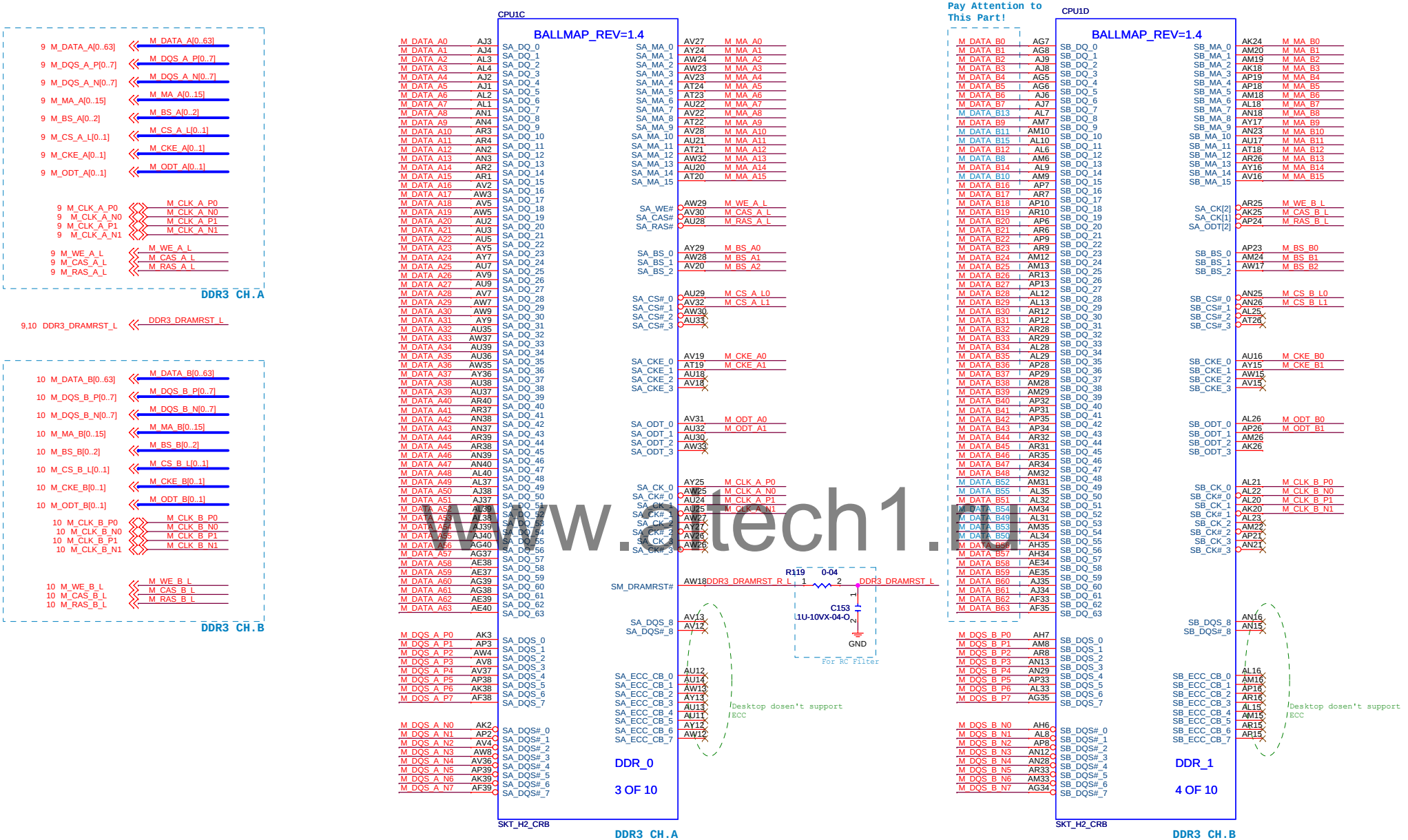

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Title	CPU - DDR3	
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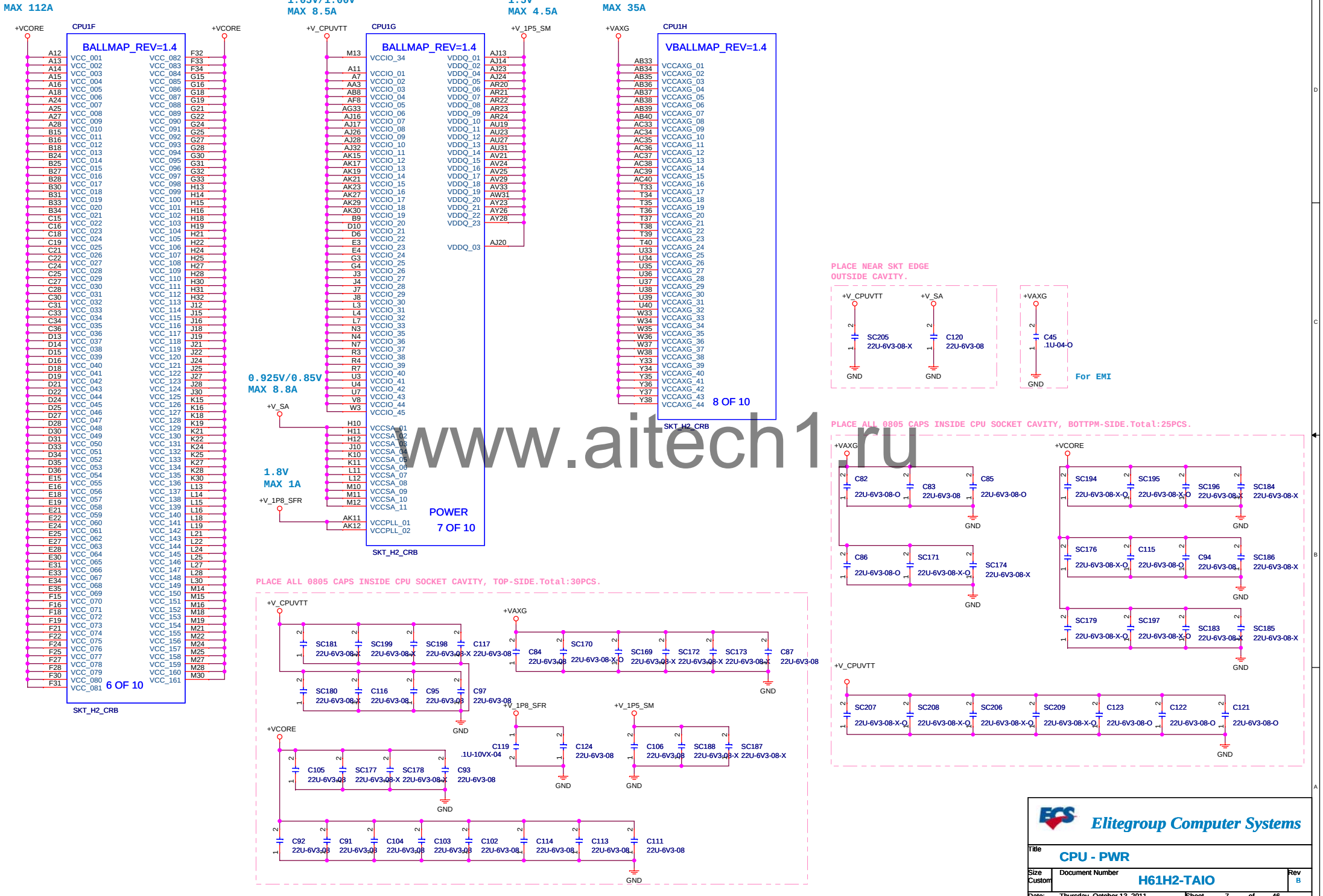

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Title: CPU - PWR

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Title: CPU - GND, CPU_RST_L

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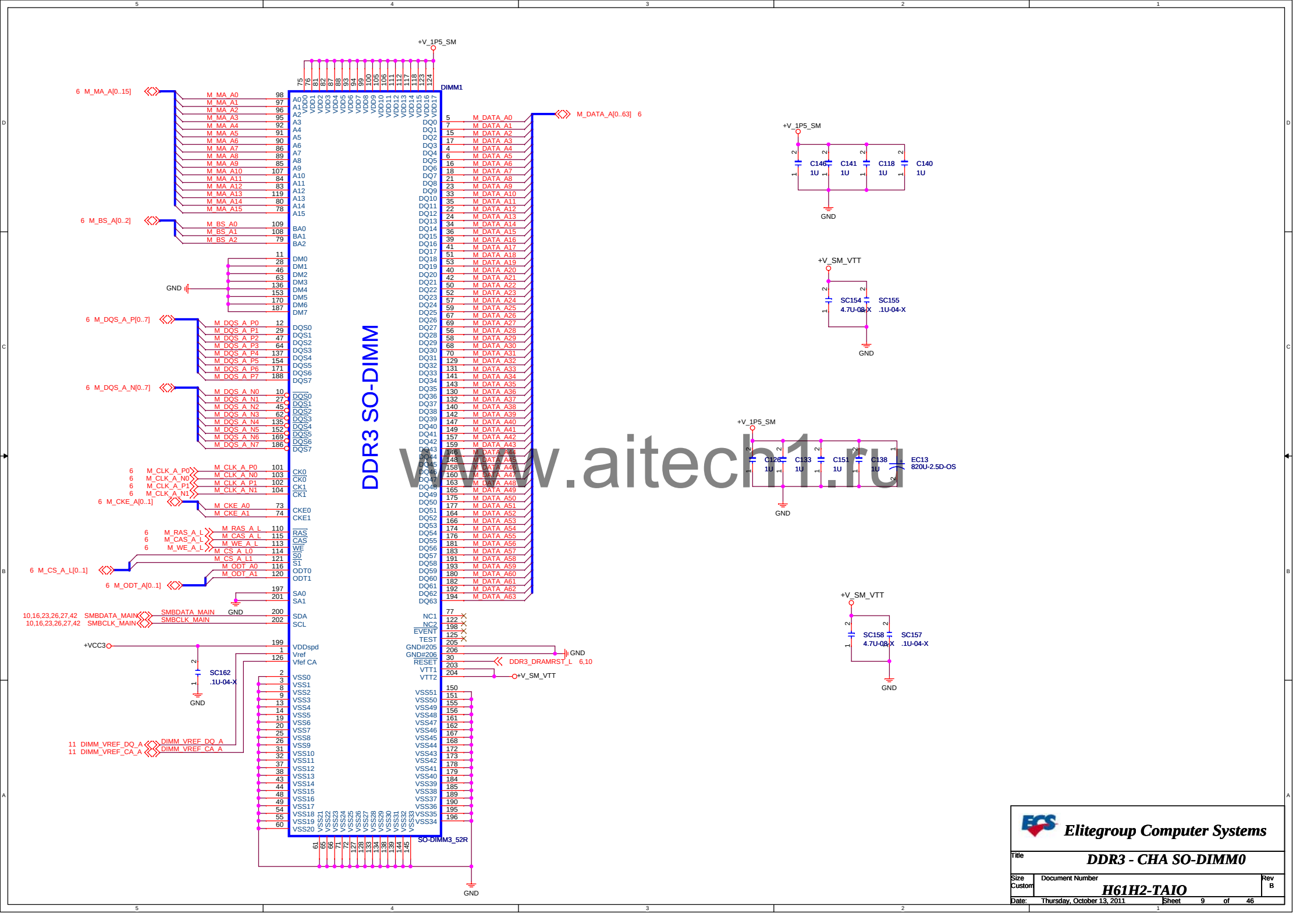

Title	DDR3 - CHA SO-DIMM0
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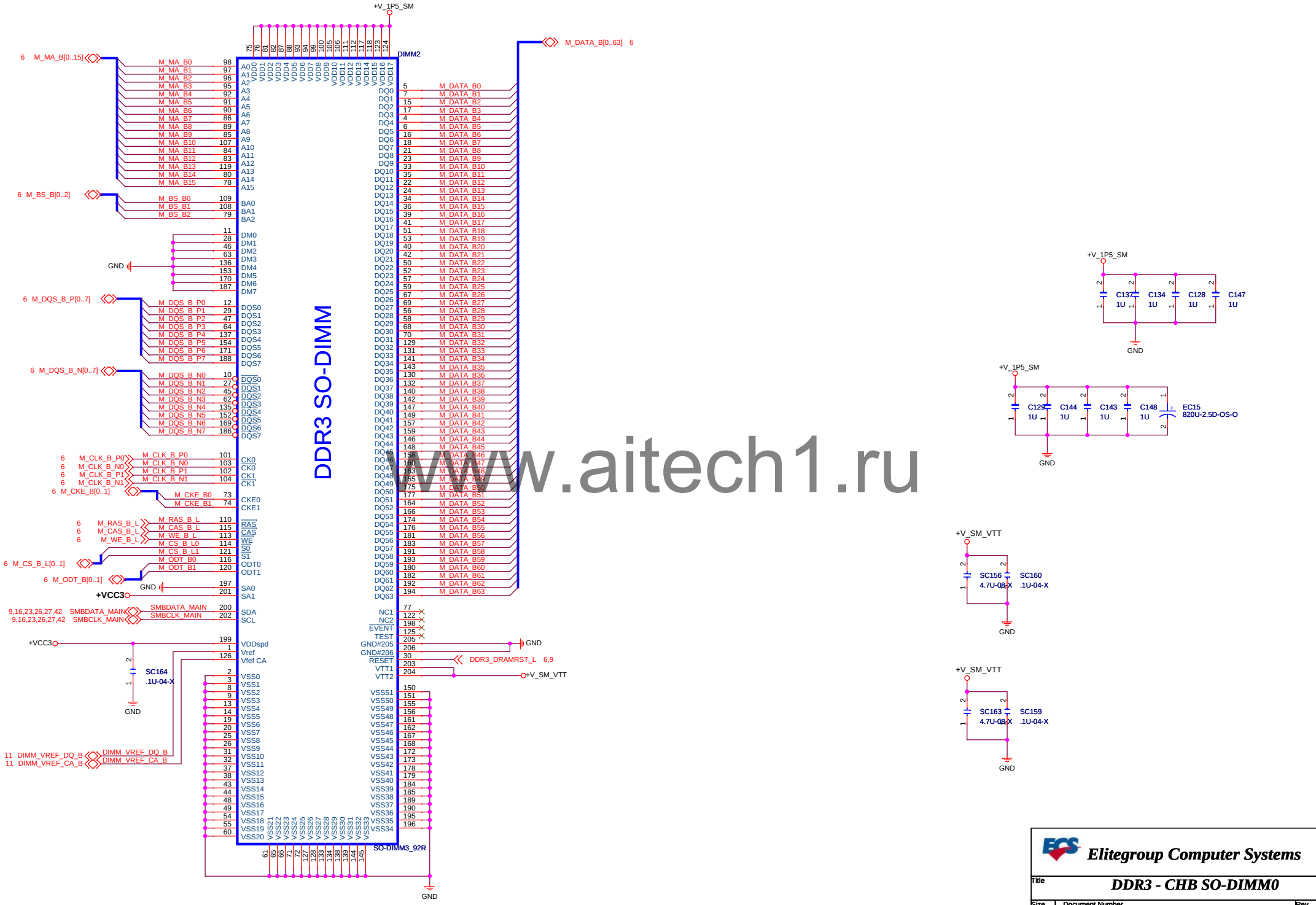

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Title	DDR3 - CHB SO-DIMM0
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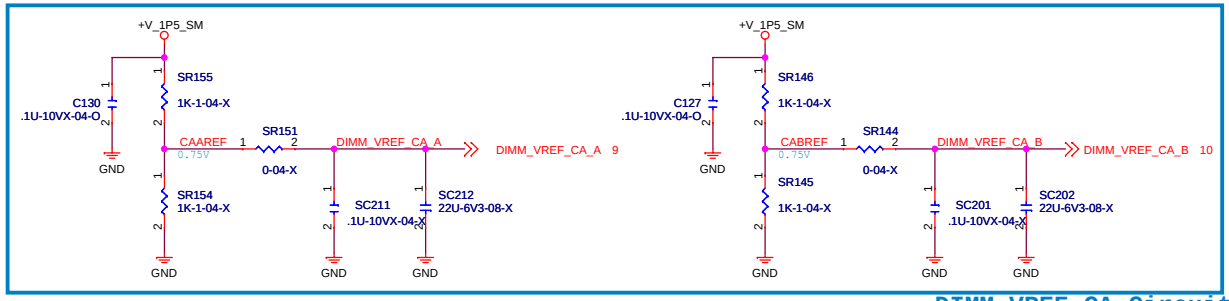
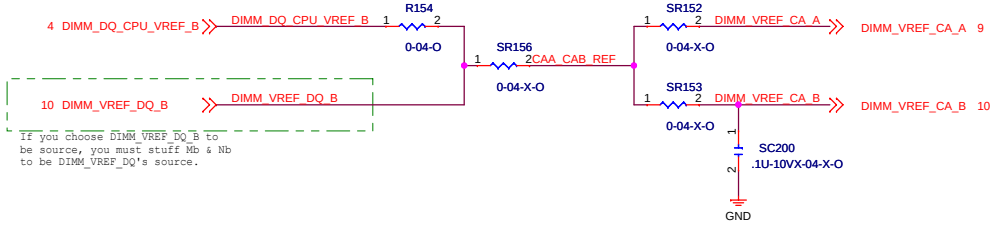
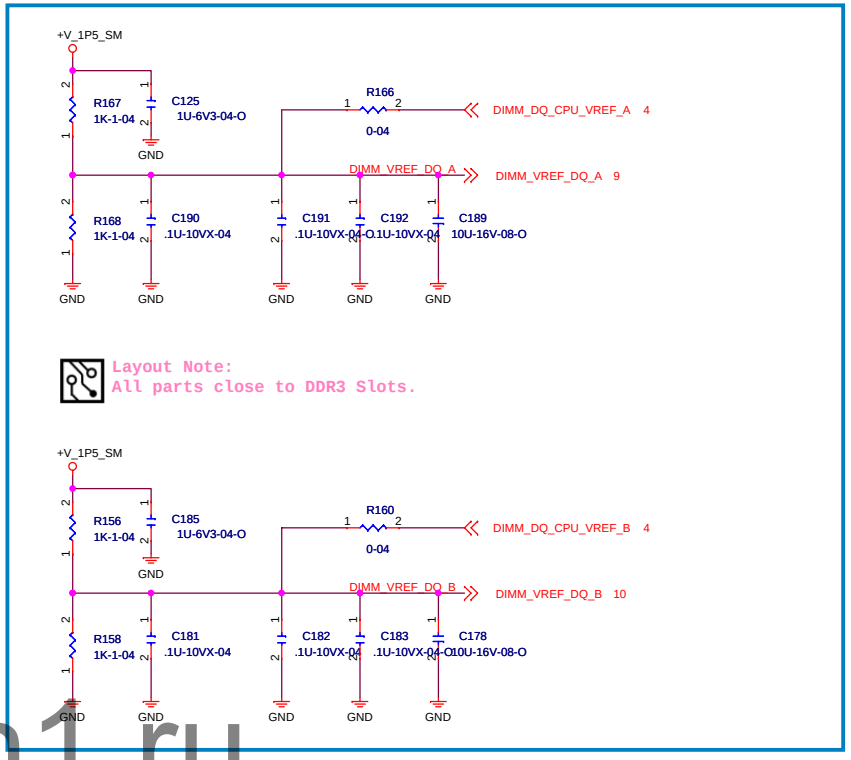
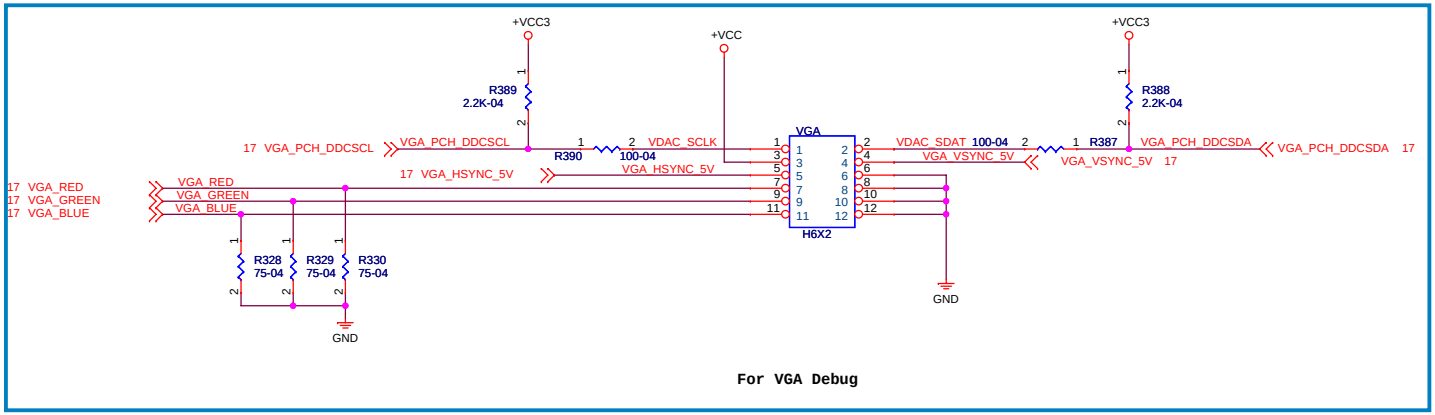


DIMM_VREF_CA Circuit





DIMM_VREF_DQ Control Circuit



For VGA Debug

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Title	DDR3 - VREF/VGA CONN	
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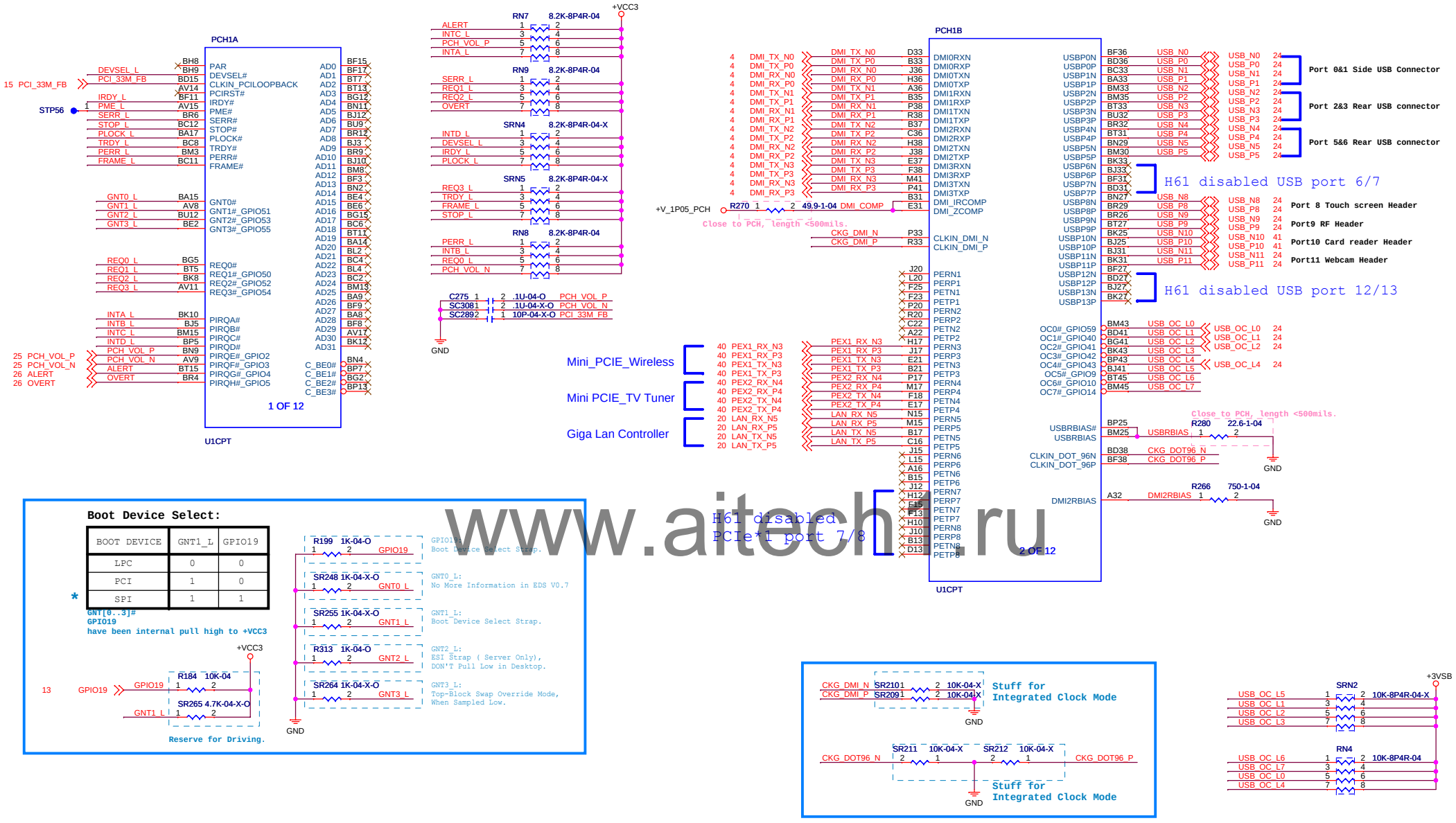

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Title: PCH_DMI/PCH_PE/USB

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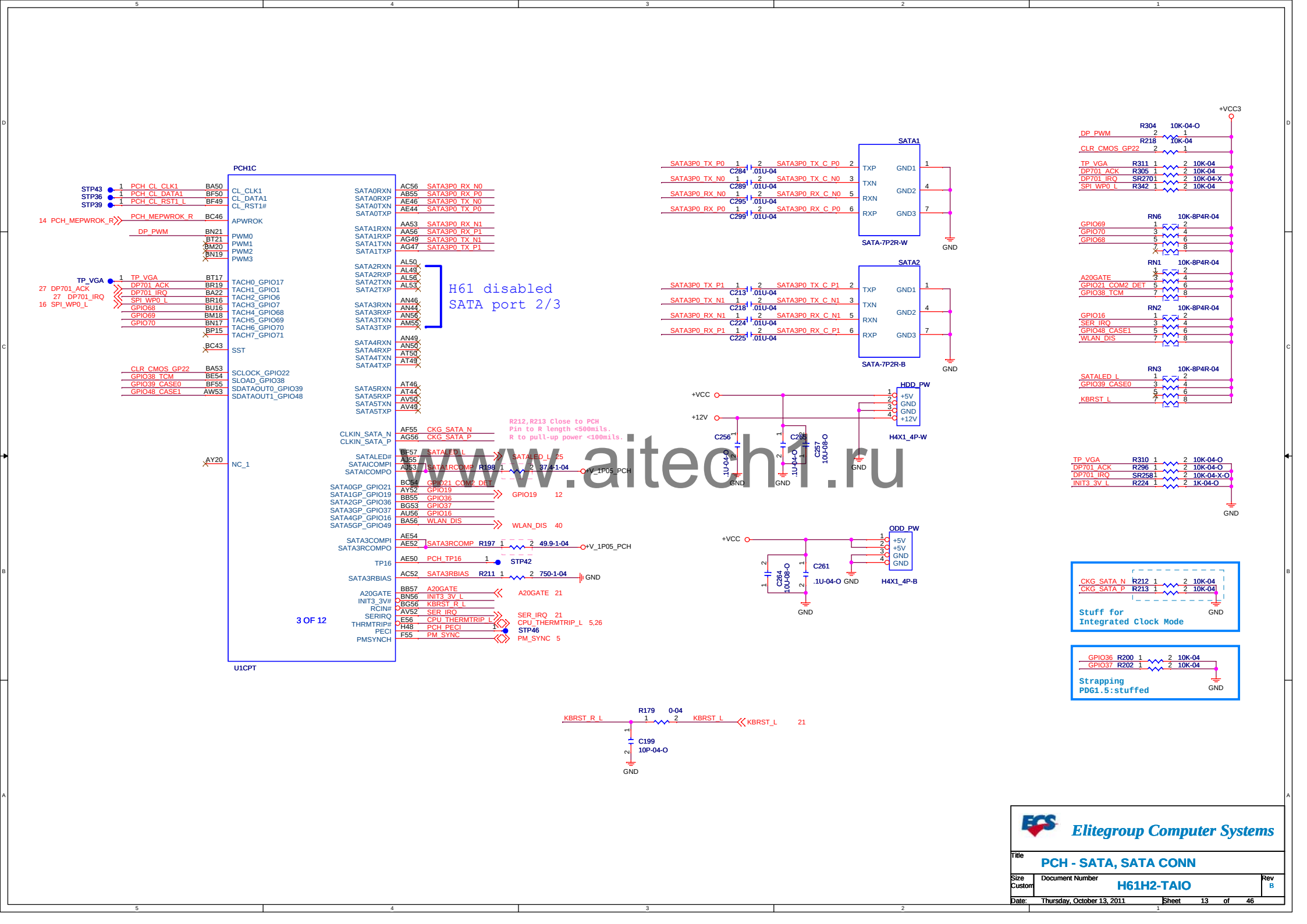
PCH1C
U1CPT
3 OF 12
H61 disabled
SATA port 2/3
R212,R213 Close to PCH
Pin to R length <500mils.
R to pull-up power <100mils.
SATA1
SATA-7P2R-W
SATA2
SATA-7P2R-B
HDD_PW
H4X1_4P-W
ODD_PW
H4X1_4P-B
Stuff for
Integrated Clock Mode
Strapping
PDG1.5:stuffed
www.aitech1.ru
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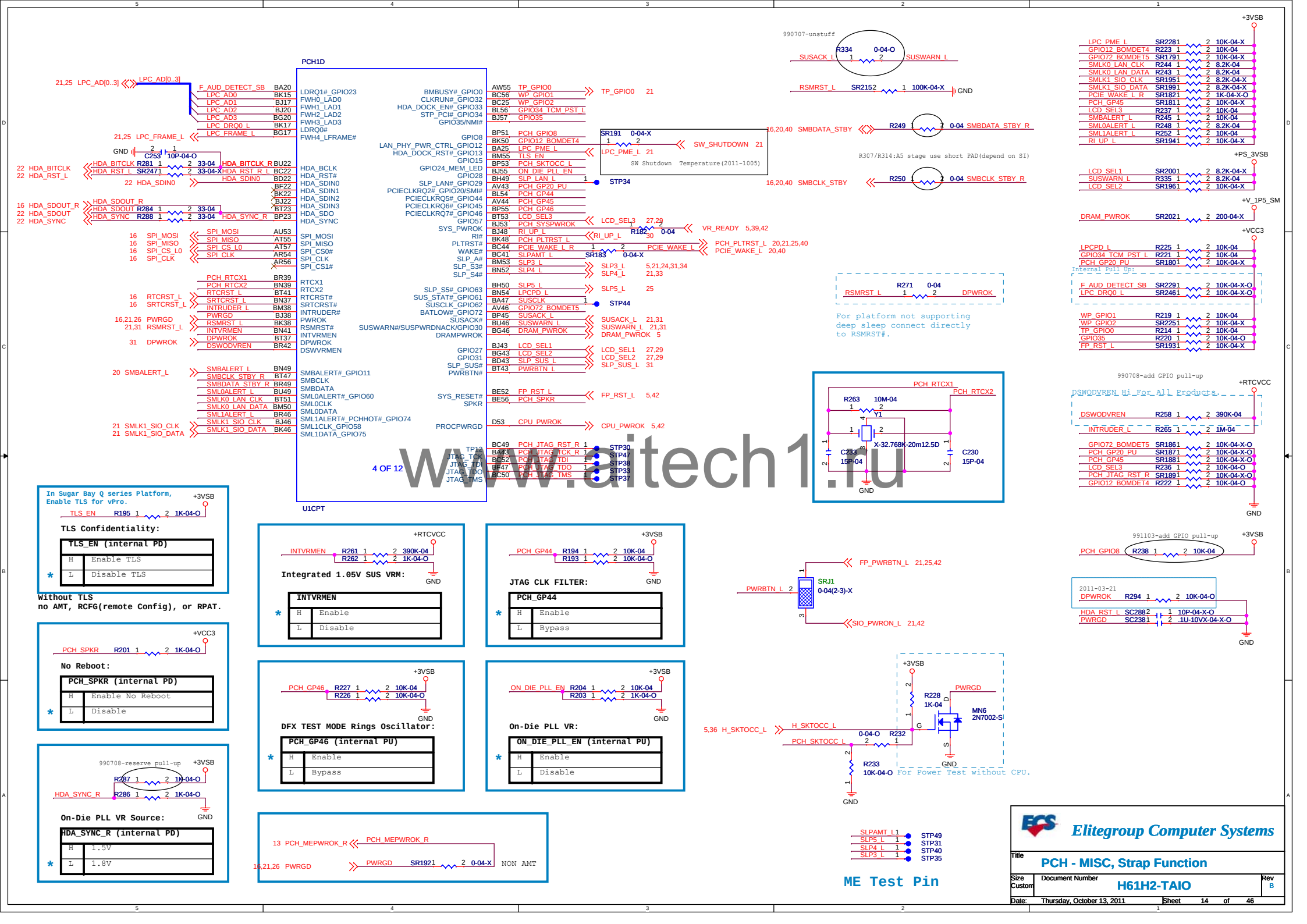

Company	Elitegroup Computer Systems
Title	PCH - MISC, Strap Function
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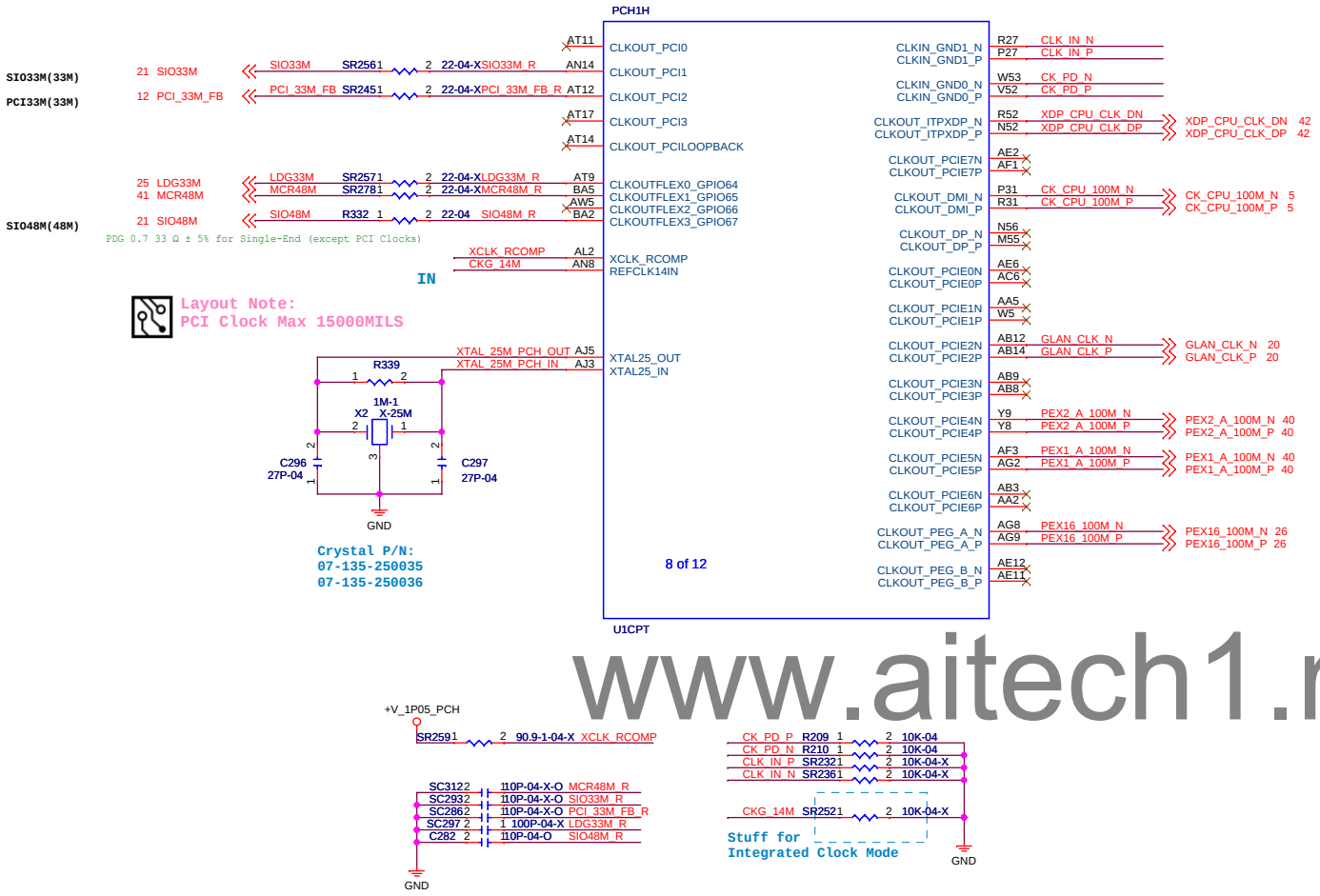

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Title	PCH - CLK IO	
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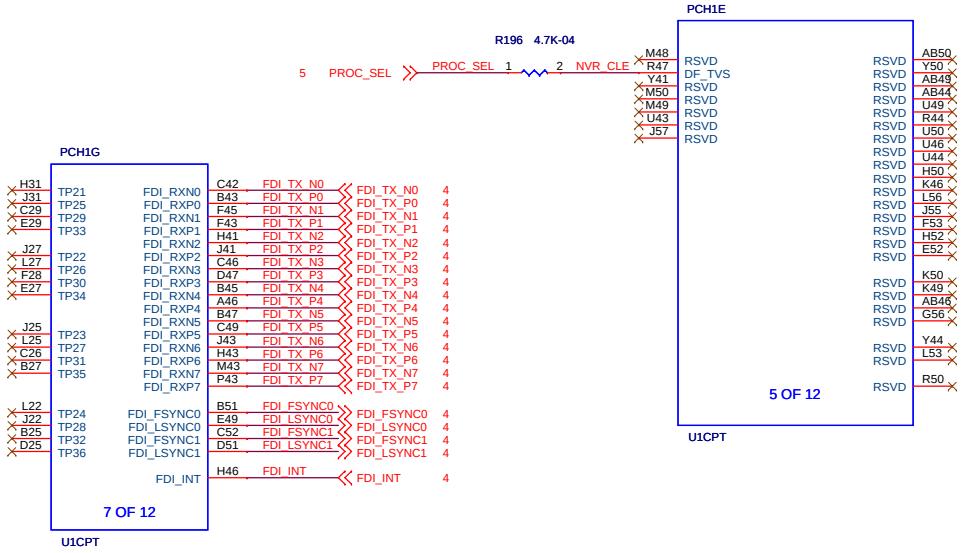
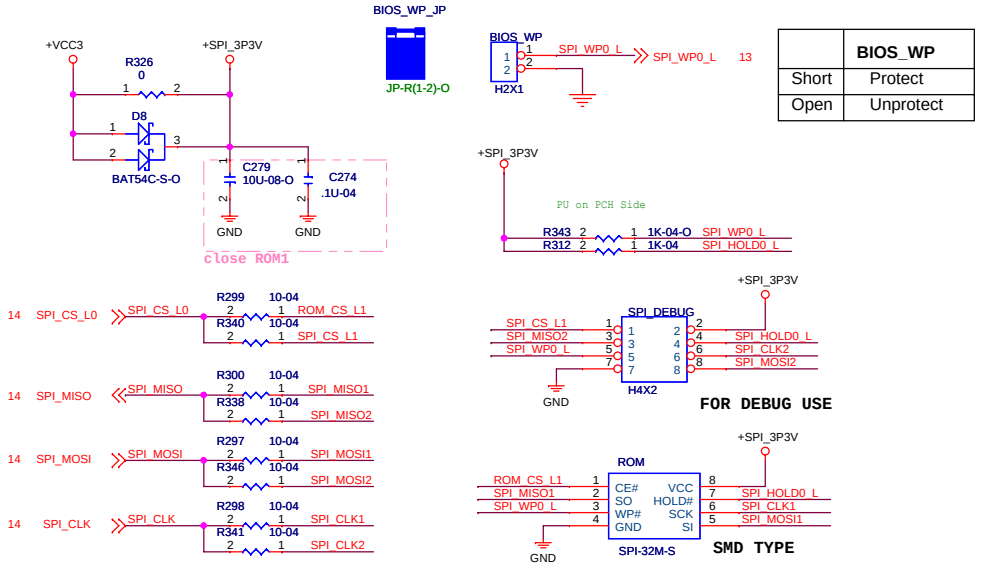
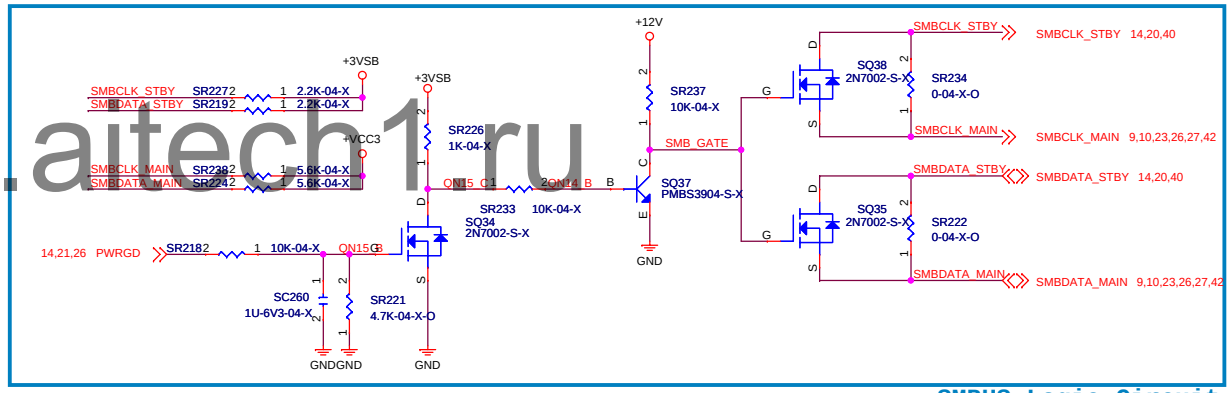


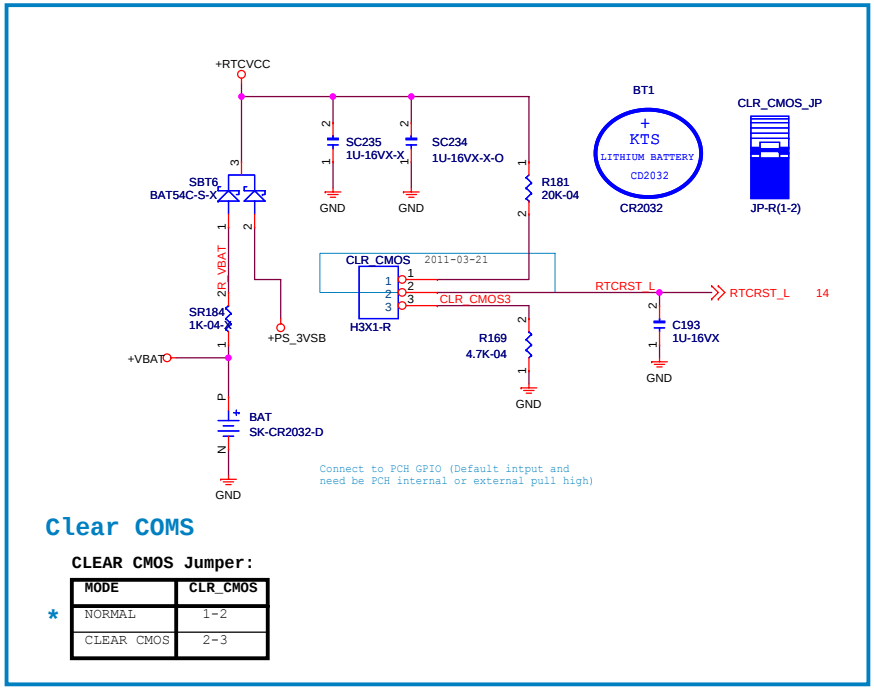


	BIOS_WP
Short	Protect
Open	Unprotect

SPI ROM Circuit



SMBUS Logic Circuit

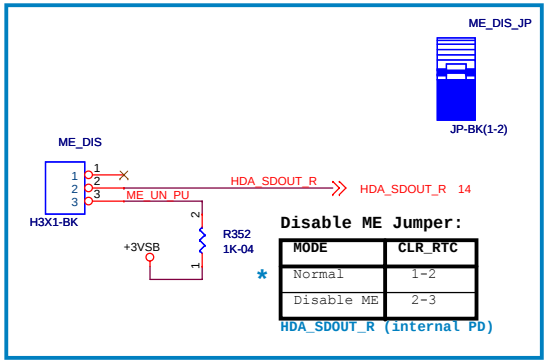


Clear COMS

CLEAR CMOS Jumper:

MODE	CLR_CMOS
NORMAL	1-2
CLEAR CMOS	2-3

*



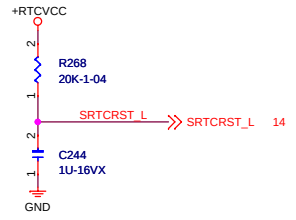
Disable ME Jumper:

MODE	CLR_RTC
Normal	1-2
Disable ME	2-3

*

HDA_SDOUT_R (internal PD)

Disable ME Header, Always Stuff for ME or non-ME Platform.



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Title	FDI,CLR_CMOS,ROM,SMbus	
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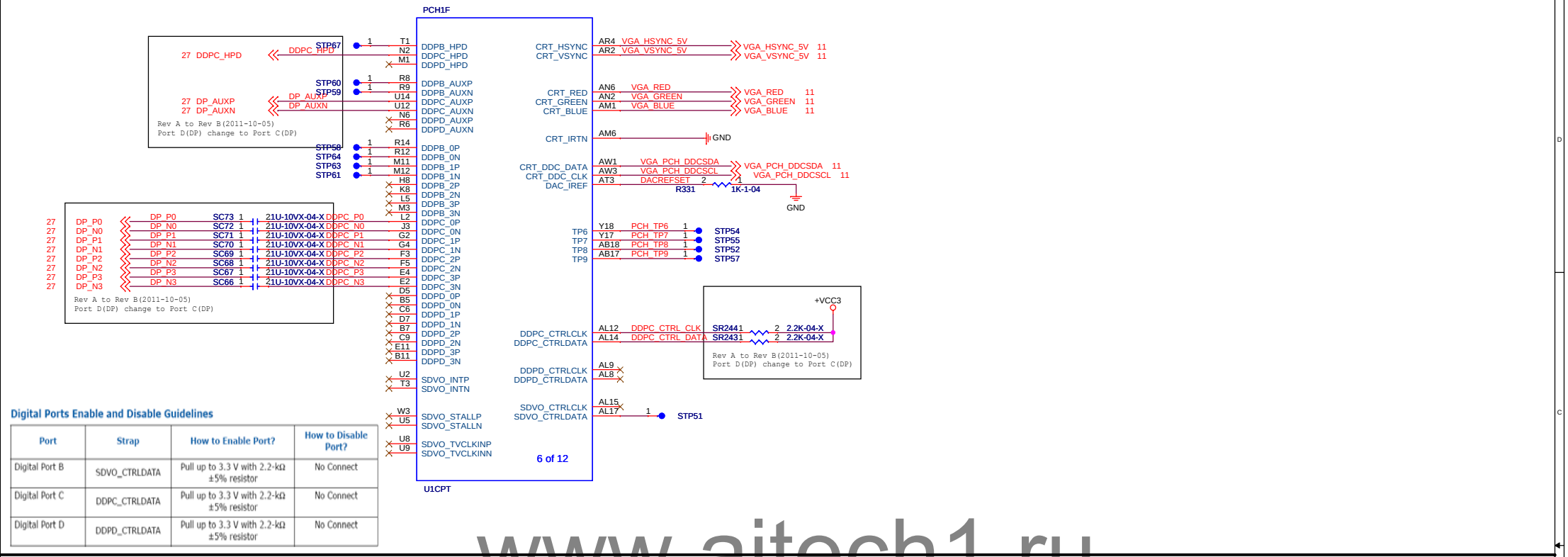

Digital Ports Enable and Disable Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Digital Port B	SDVO_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Digital Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Digital Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

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Title: PCH - HDMI/VGA

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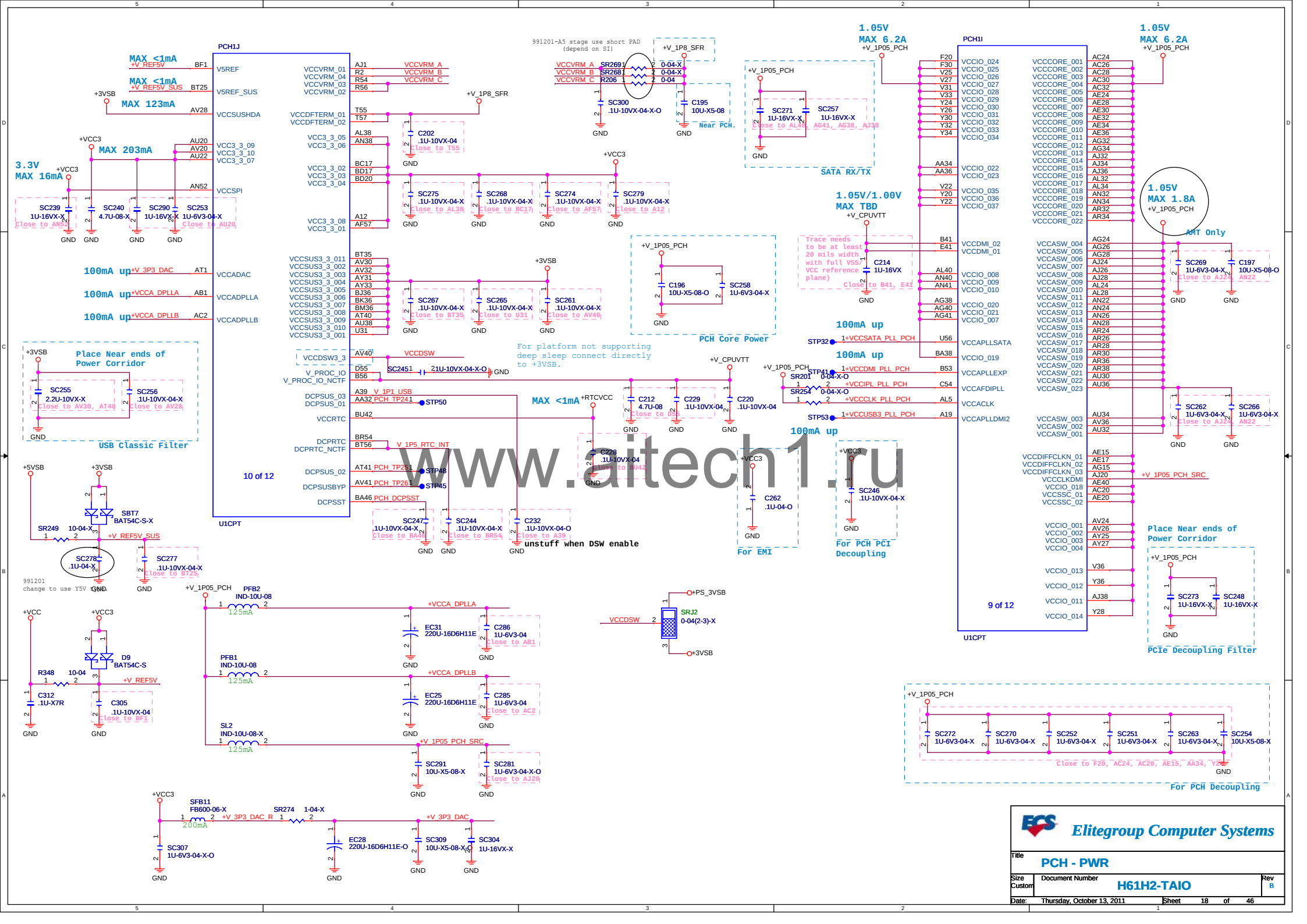

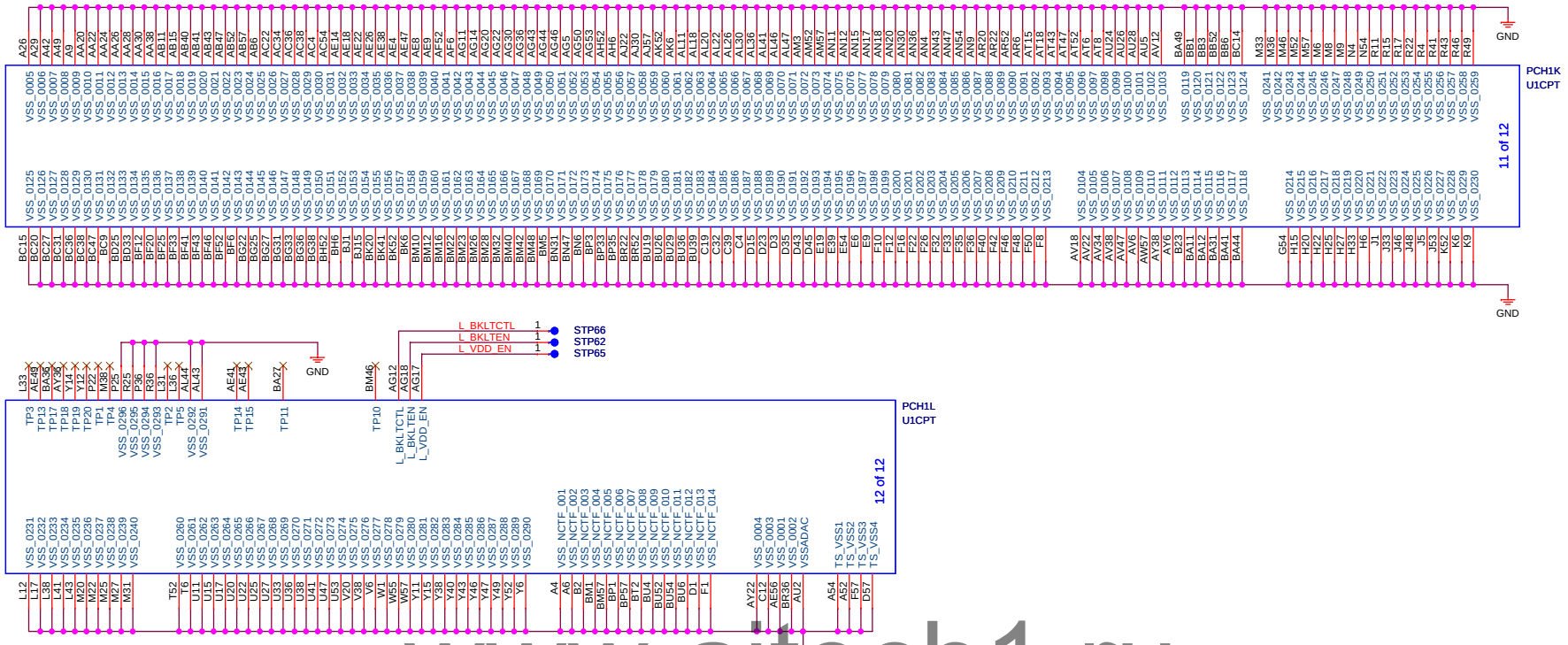

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Title	PCH - GND		
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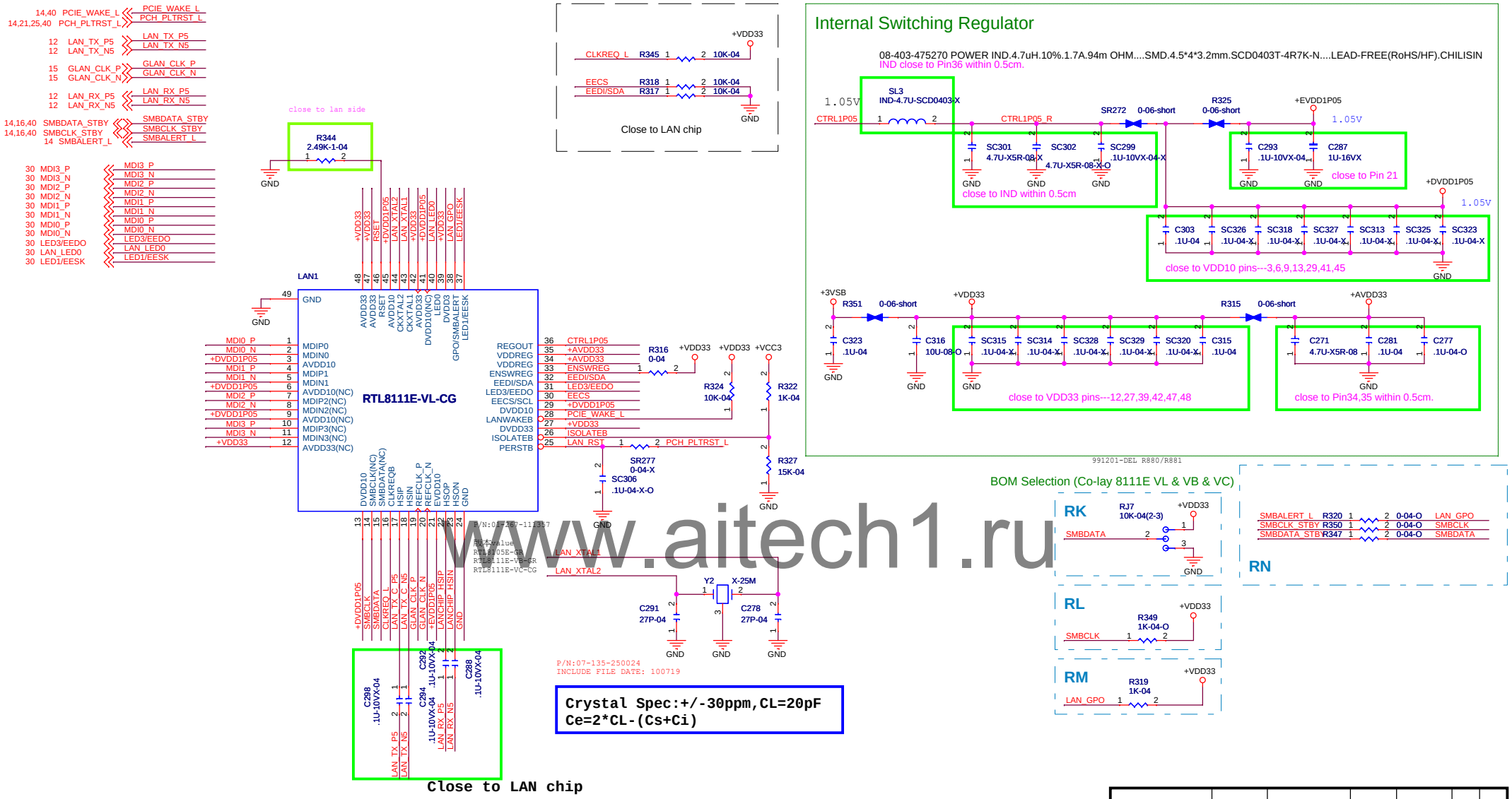

For China-one LED Light:

	Status	Yellow	Grn/Org
	No Link	Off	Off
	S3/S4/S5	Off	Off
	10M, inactive	Off	Off
	10M, active		Off
	100M, inactive	Off	
	100M, active		
	1G, inactive	Off	
	1G, active		
	Blinking		

Chip/version		ASF	EEPROM	RM	RK	RL	RN
8111E	VL	Without ASF	EEPROM (93C46)	O	10K GND	X	X
			EEPROM (93C56/66)	O	1K VDD33	X	X
			EFUSE	O	10K GND	X	X
	VB,VC	With ASF	EEPROM (93C66)	O	1K VDD33	O	O

*It must be used external EEPROM(93C66) that support ASF.

<OrgAddr1> Elitegroup Computer Systems

Title: LAN(RTL8105E/8111E)

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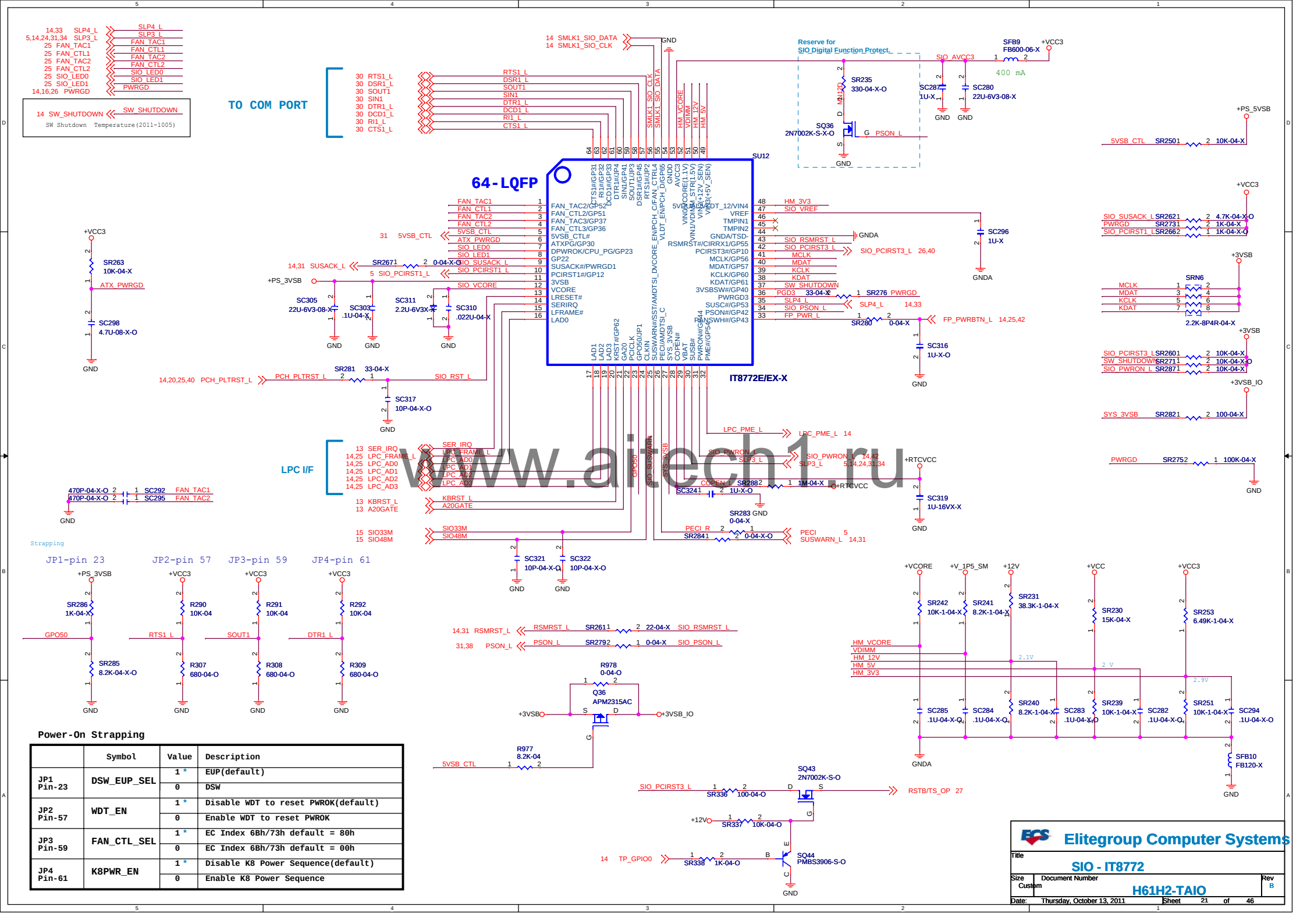
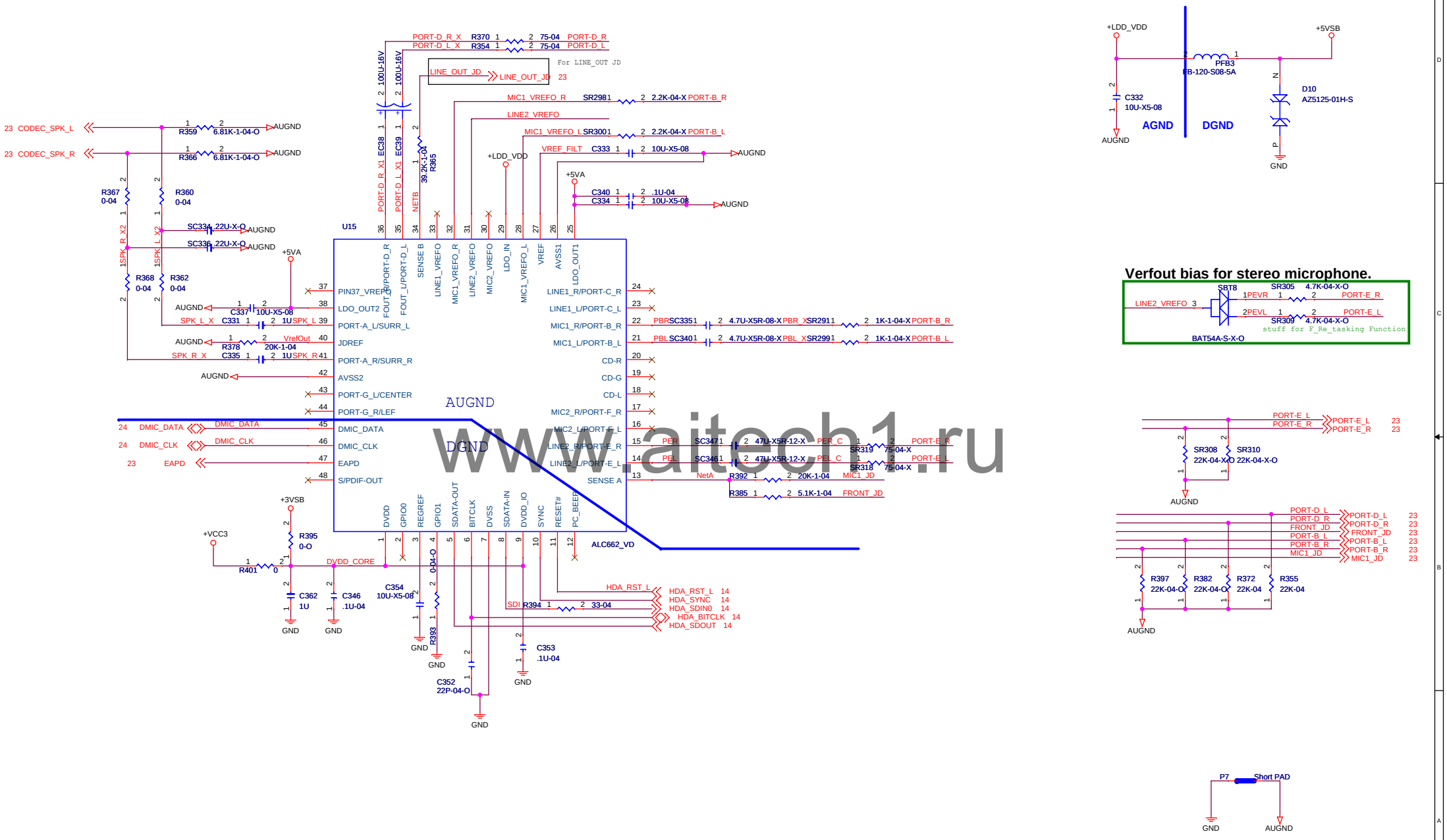
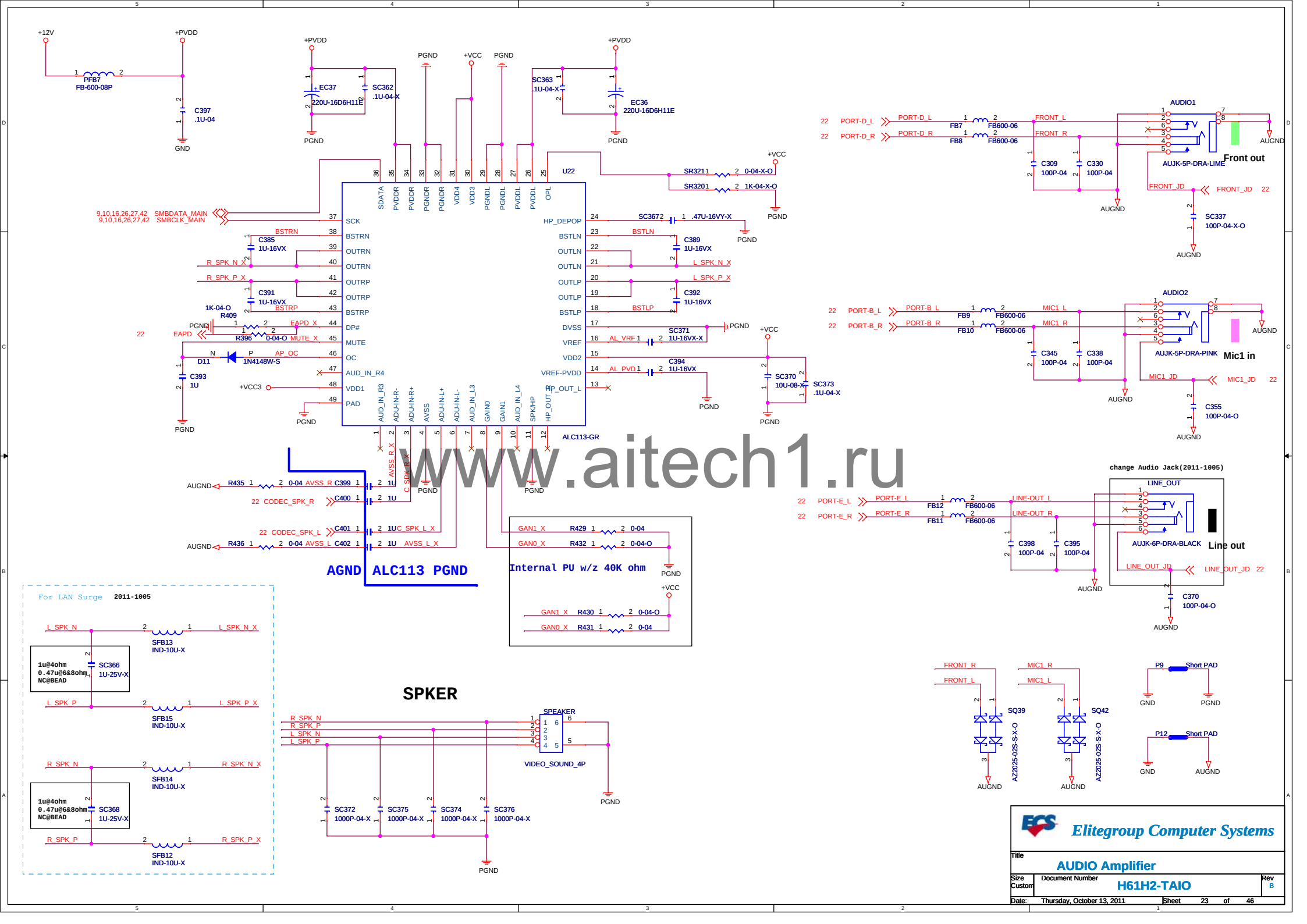


	Symbol	Value	Description
JP1 Pin-23	DSW_EUP_SEL	1 *	EUP(default)
		0	DSW
JP2 Pin-57	WDT_EN	1 *	Disable WDT to reset PWROK(default)
		0	Enable WDT to reset PWROK
JP3 Pin-59	FAN_CTL_SEL	1 *	EC Index 6Bh/73h default = 80h
		0	EC Index 6Bh/73h default = 00h
JP4 Pin-61	K8PWR_EN	1 *	Disable K8 Power Sequence(default)
		0	Enable K8 Power Sequence





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Title: AUDIO Amplifier

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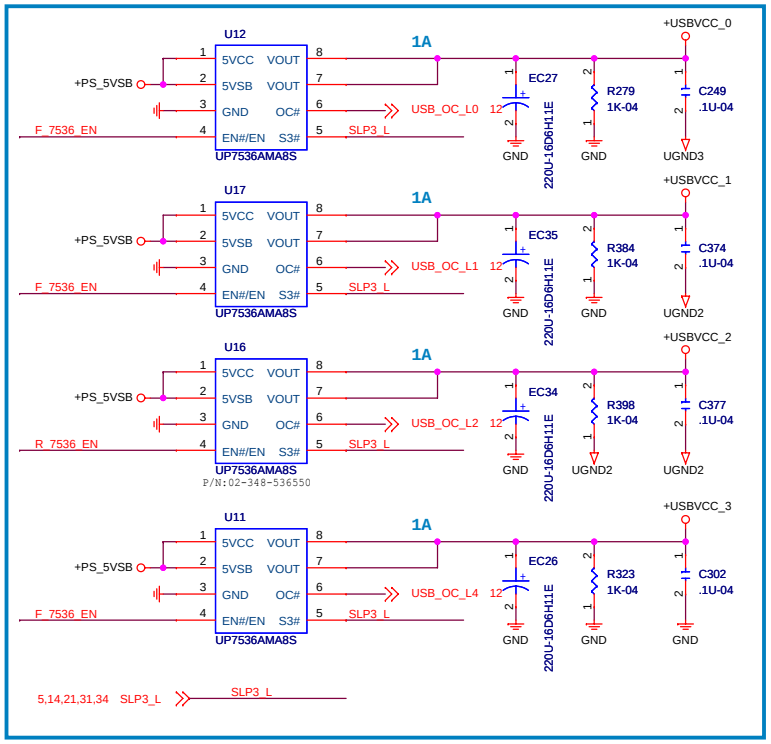
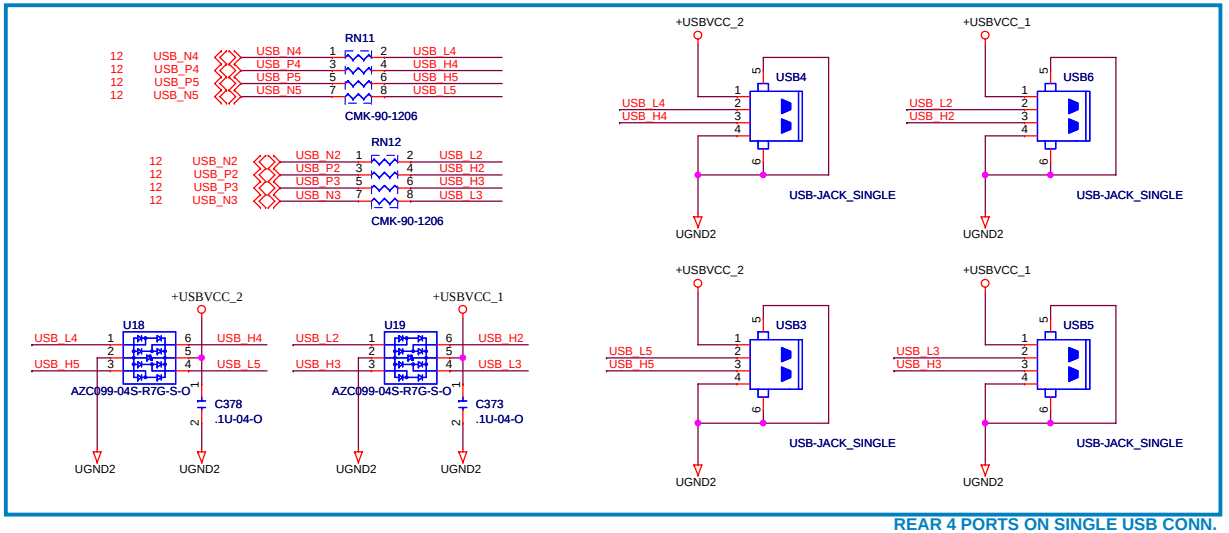
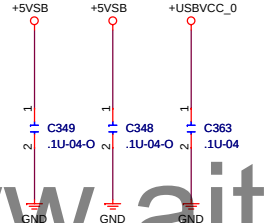
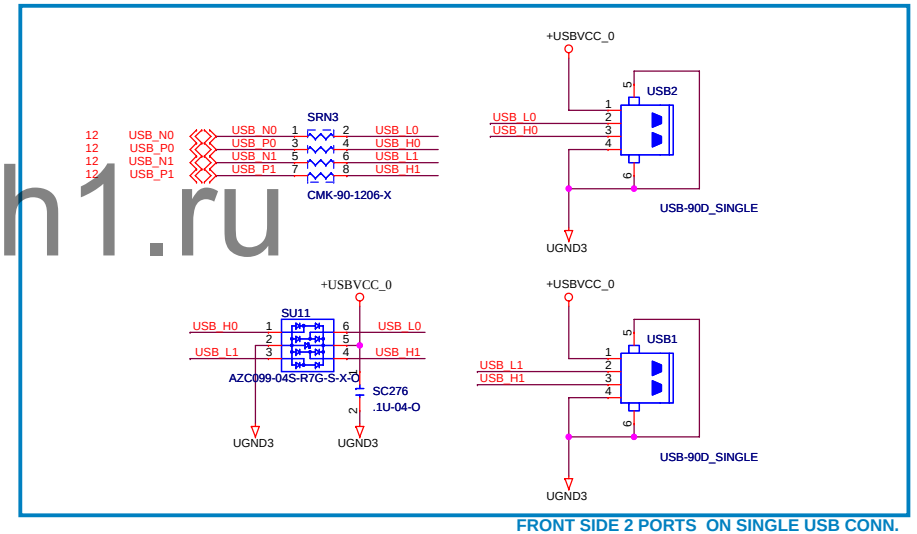


USB POWER CIRCUIT

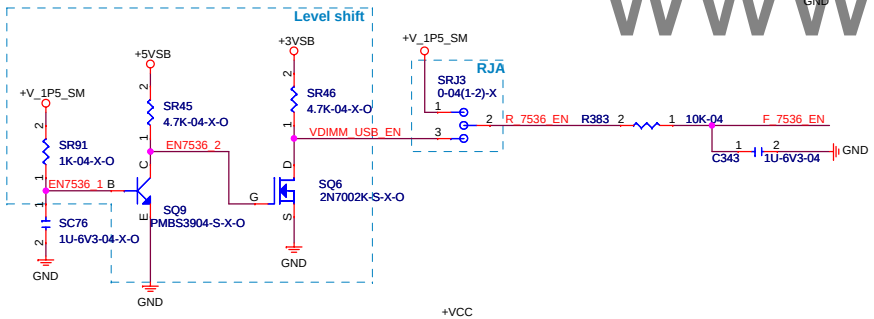


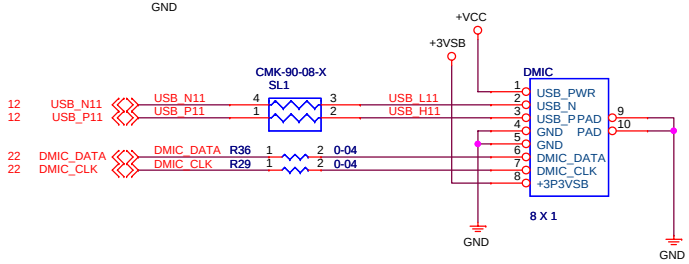
REAR 4 PORTS ON SINGLE USB CONN.

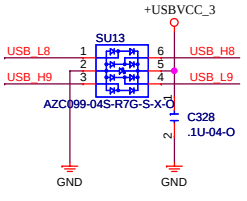


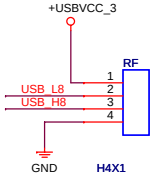


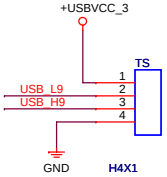
FRONT SIDE 2 PORTS ON SINGLE USB CONN.

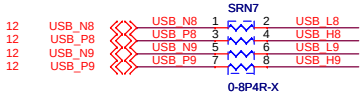


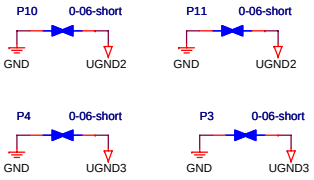












uP7536 Enable use	Level shift	RJA	RJB	S4/S5 USB_5V_DUAL	Customer
* VDIMM	N A	0ohm (1-2)	N A	0 Volt	Lenovo S4/S5 w/o USB_5V_DUAL
VDIMM level shift (3.3V)	Stuff	0ohm (2-3)	N A	0 Volt	

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Title: USB - PWR/CONN/HDR

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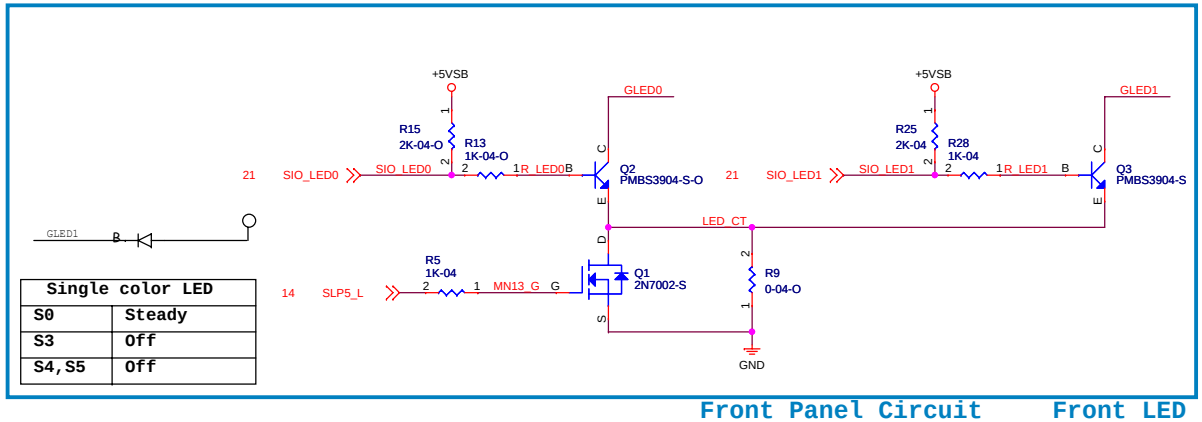
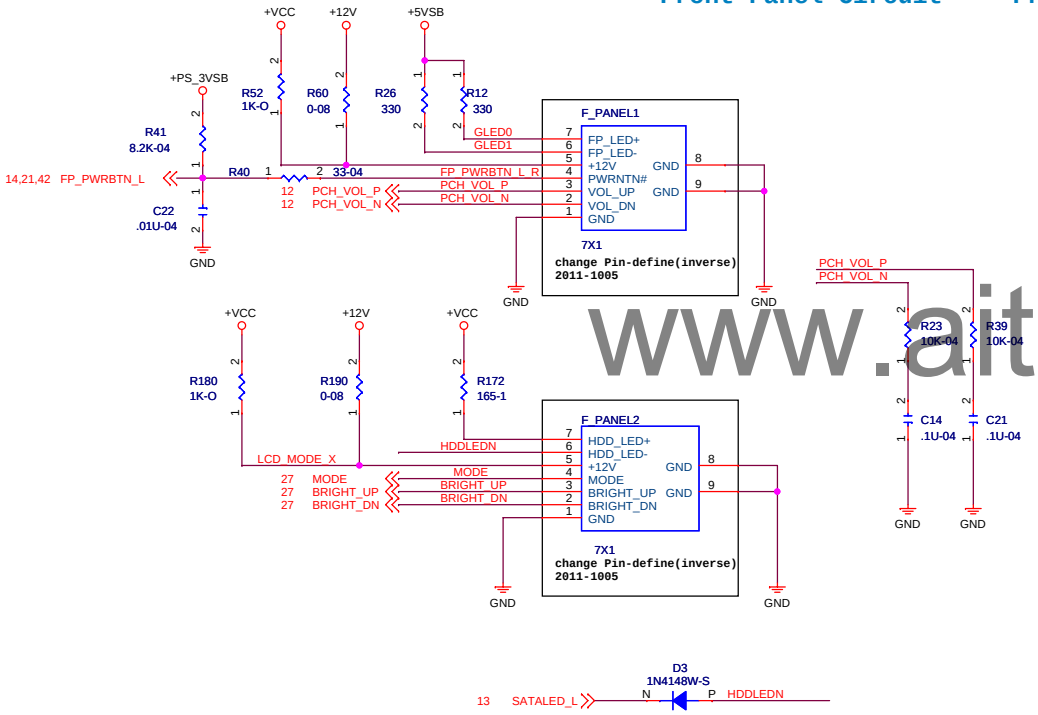
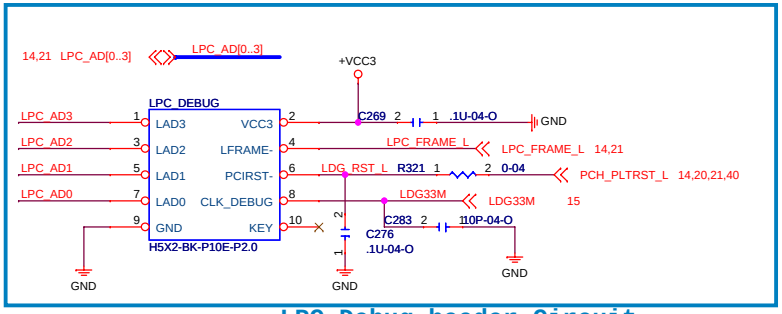
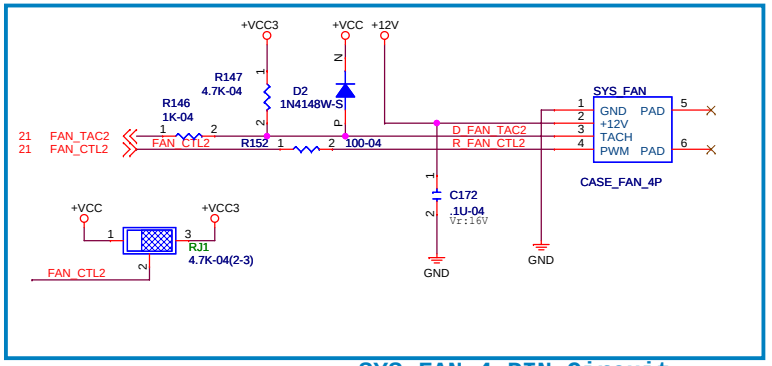


Front Panel Circuit Front LED

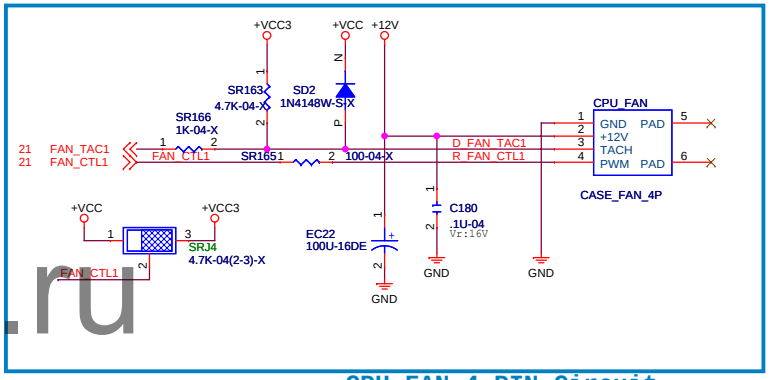




LPC Debug header Circuit



SYS FAN 4-PIN Circuit



CPU FAN 4-PIN Circuit

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Title: LPC Device/FAN/F_PANEL

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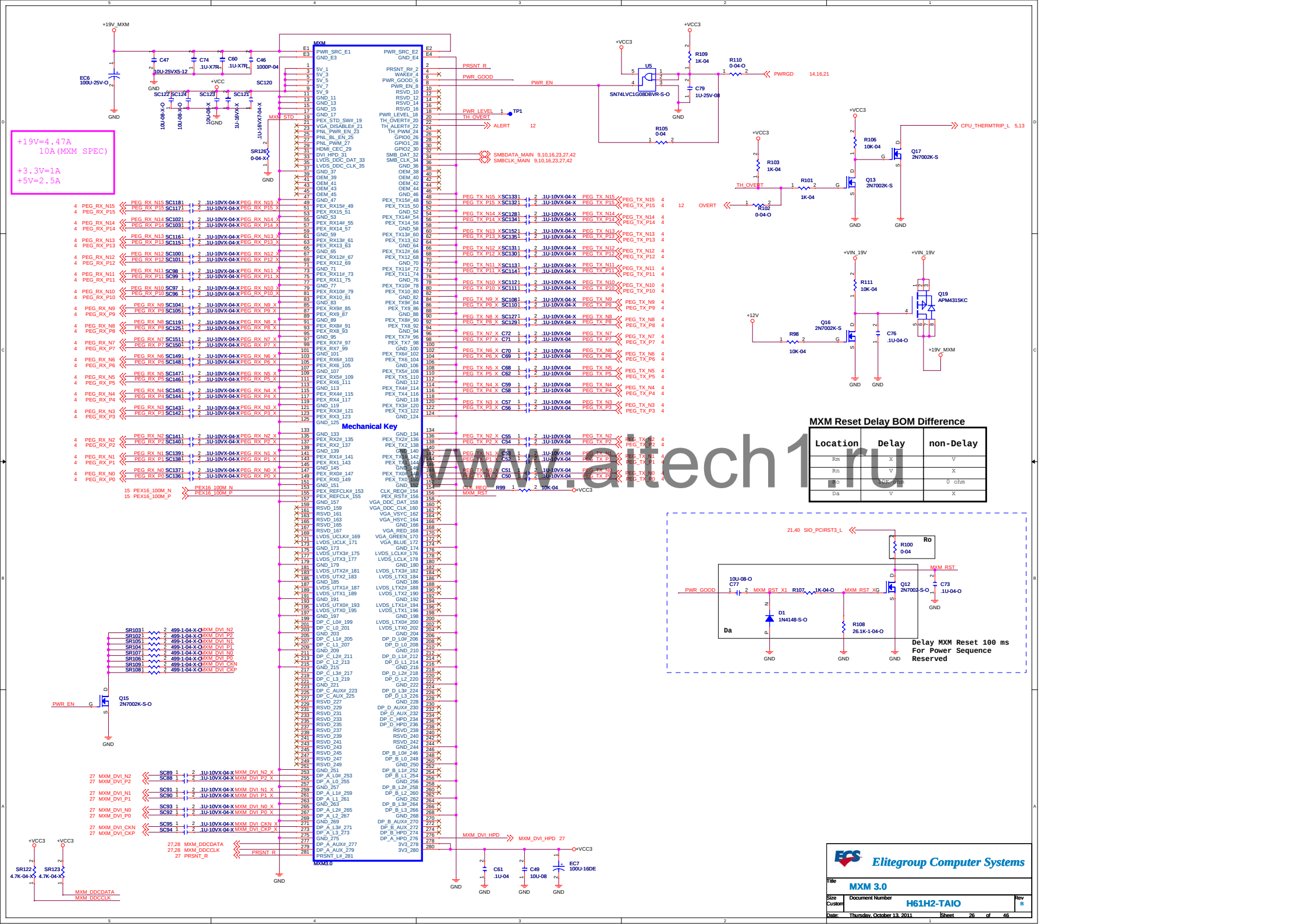

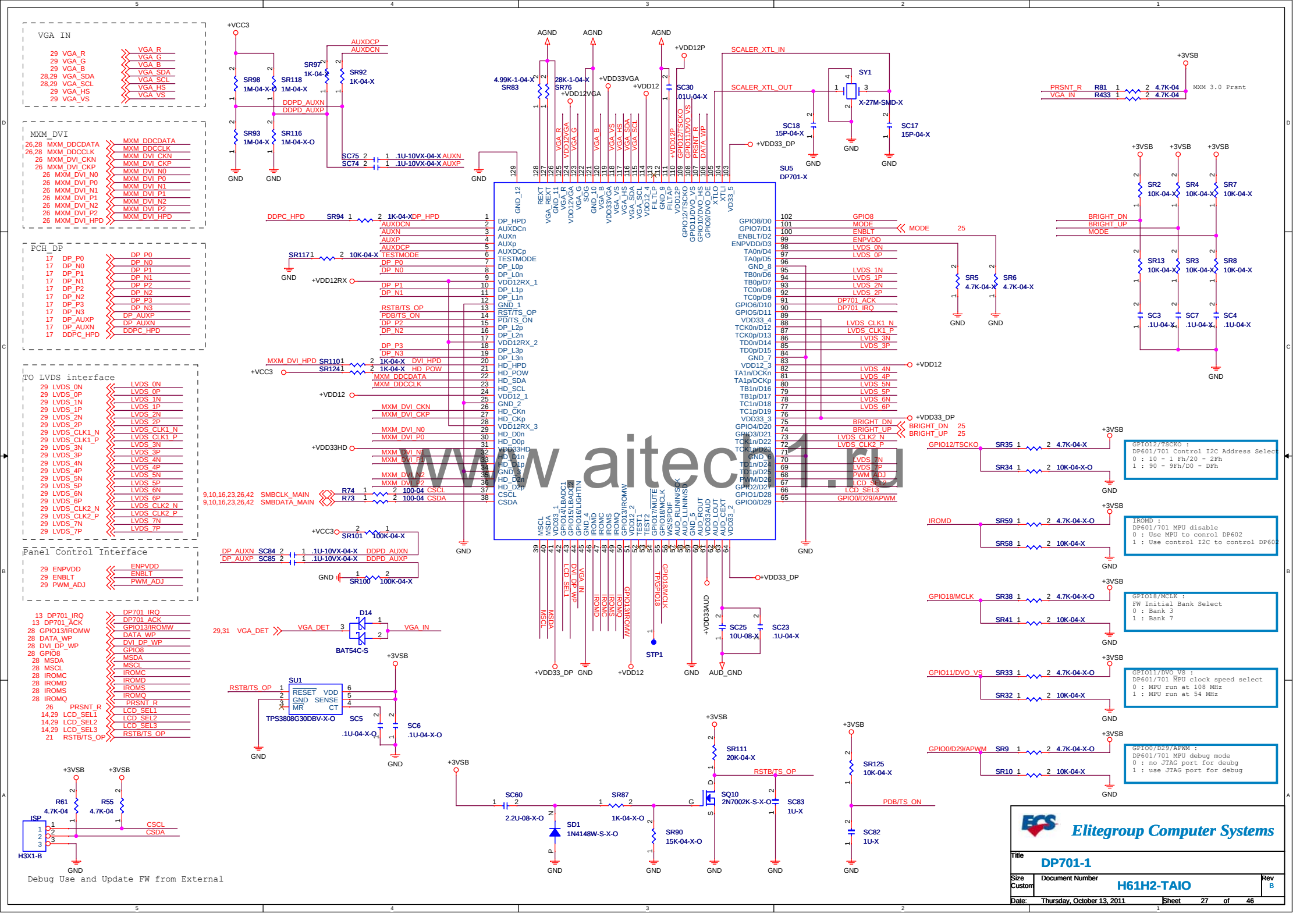

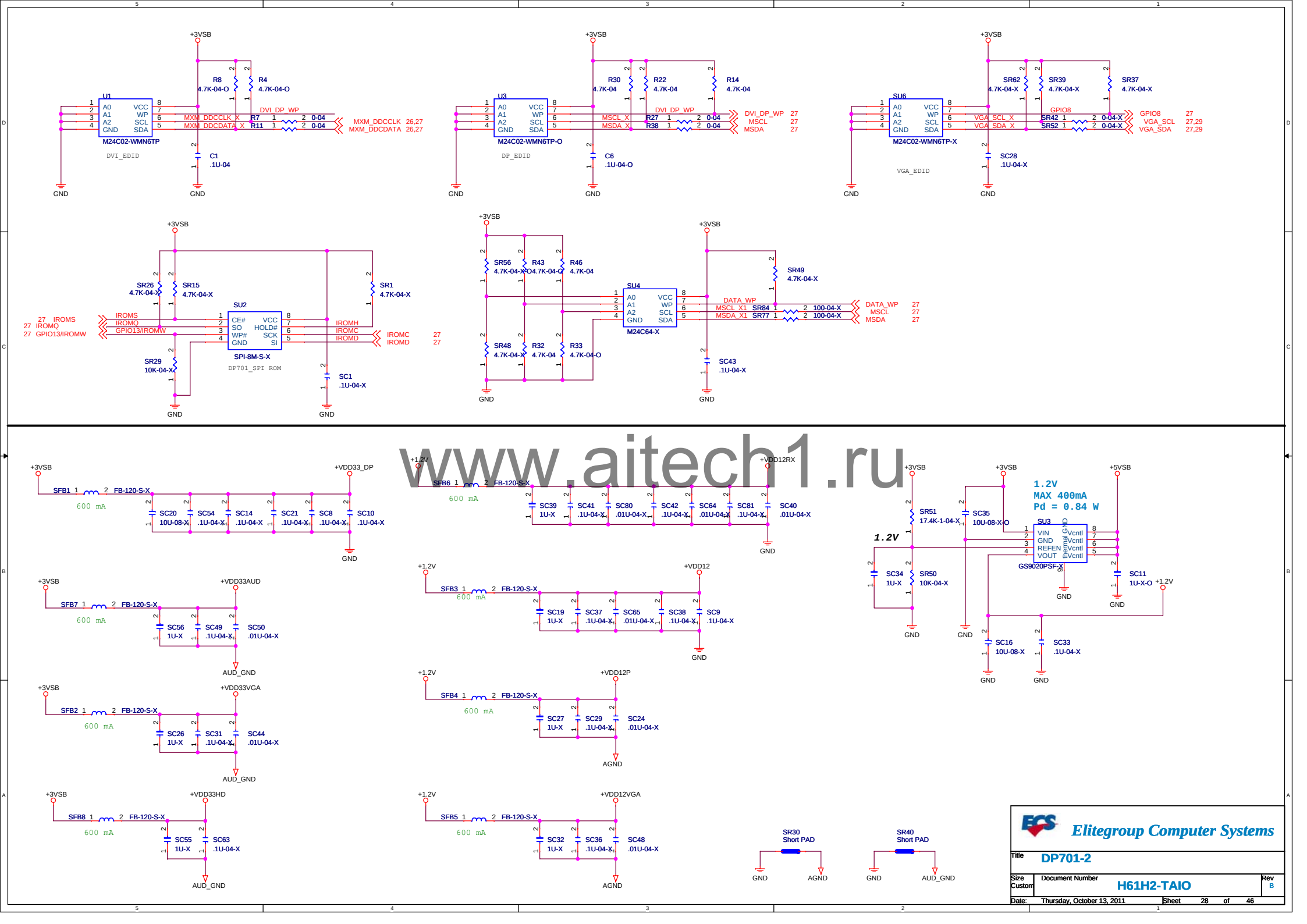

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Title	DP701-2	
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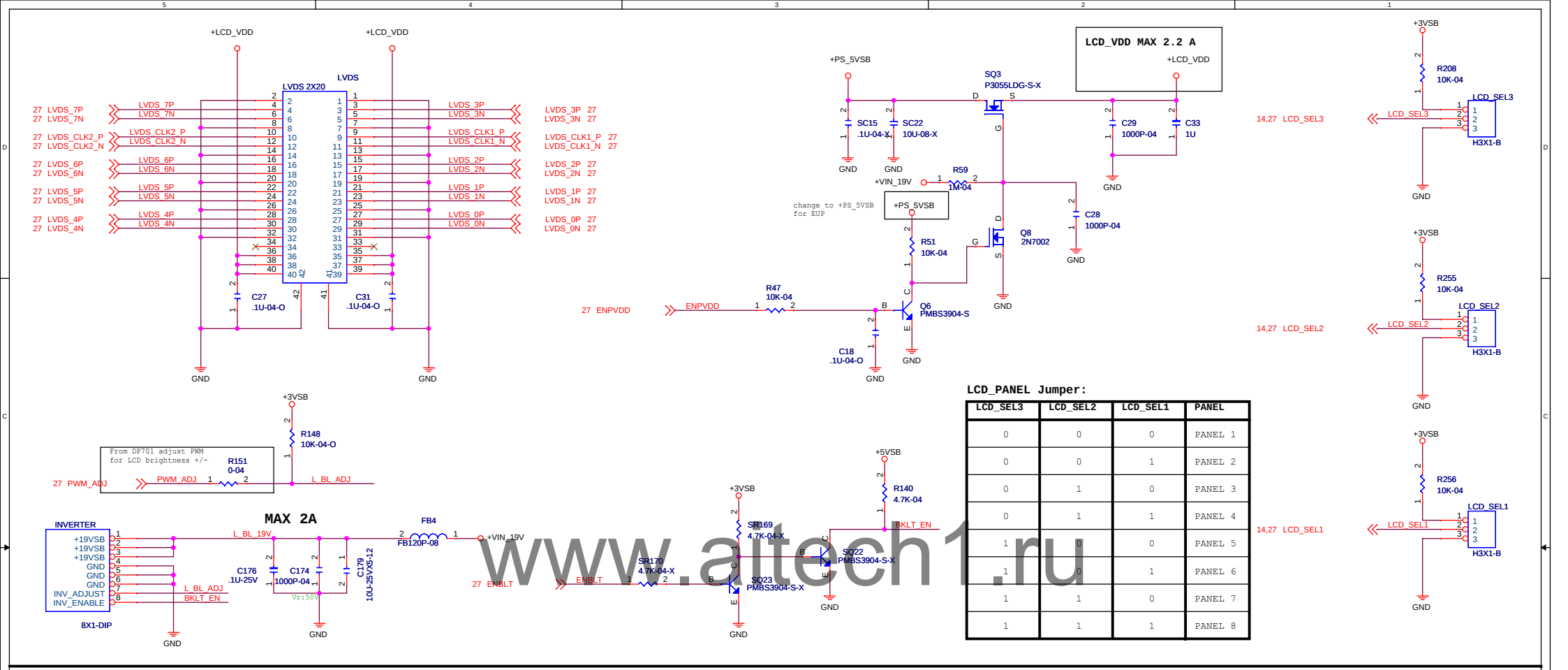
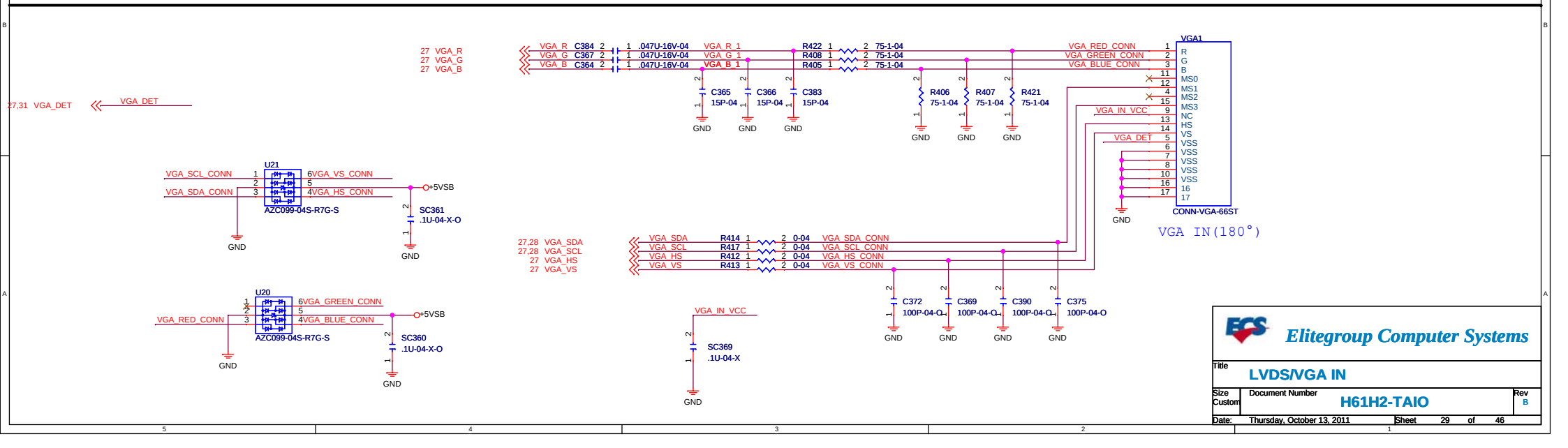


LCD_PANEL Jumper:

LCD_SEL3	LCD_SEL2	LCD_SEL1	PANEL
0	0	0	PANEL 1
0	0	1	PANEL 2
0	1	0	PANEL 3
0	1	1	PANEL 4
1	0	0	PANEL 5
1	0	1	PANEL 6
1	1	0	PANEL 7
1	1	1	PANEL 8



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Title: LVDS/VGA IN

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COM Port

21 DCD1_L
21 RI1_L
21 CTS1_L
21 DTR1_L
21 RTS1_L
21 DSR1_L
21 SOUT1
21 SIN1

COM

SU10 MAX3243_SSOP28-X

SC249 .47U-16VY-X
SC250 .47U-16VY-X
SC259 .1U-X7R
SC264 .47U-16VY-X
C250 .1U-25V
R285 10K-04

COM_V- COM_C2+ COM_C2- COM_V+ COM_C1+ COM_C1-
DCD1_L RI1_L SIN1 RTS1_L SOUT1 CTS1_L DTR1_L DSR1_L
NDCDB NRIB NSINB NRTSB NSOUTB NCTSB NDTRB NDSRB
COM_F-OFF COM_F-ON
+VCC GND

COM
H5X2-P10E-GR

CN1 CN2 180P-8P4C

PCH
R269 10K-04-O
R_NRI
QN5 PMBS3904-S-O
R283 10K-04-O
C251 1U-6V3-04-O
C260 1000P-04-O
RI_UP_L

COM RI# Wake Up Circuit

U14 TRANSFORMER

MDI3_N MDI3_P MDI2_N MDI2_P MDI1_N MDI1_P MDI0_N MDI0_P
TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-
CMT1 TX1+ TX1- CMT2 TX2+ TX2- CMT3 TX3+ TX3- CMT4 TX4+ TX4-
LAN_MDI3_N LAN_MDI3_P LAN_MDI2_N LAN_MDI2_P LAN_MDI1_N LAN_MDI1_P LAN_MDI0_N LAN_MDI0_P

C325 .01U-04
SRN10 75-8P4R-X
C371 C376 C380 C382 1000P-2KV-12-X-O
SC359 1000P-2KV-12-X

SRN9 SRN8 0-8P4R-X

SU18 SU17 AZ3028-04P-X-O

LED3/EEDO LAN_LED0 LED1/EESK

LAN RJ45_TRANS
-LINK_1G -LINK_100 ACTIVE_P
R410 150 LED1/EESK
R411 150 LAN_LED0
R416 330 LED3/EEDO
+VDD33
C368 C351 C350 470P-O
UGND1

SU14 SU15 AZ1013-04S-X-O
C326 SC3301 .1U-04-O

SU19 SU20 AZ3033-04P-X

SR3341 SR3391 SR3351 0-08-X

P8 0-06-short

GND +VDD33 UGND1

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Title	COM PORT/LAN CONN	
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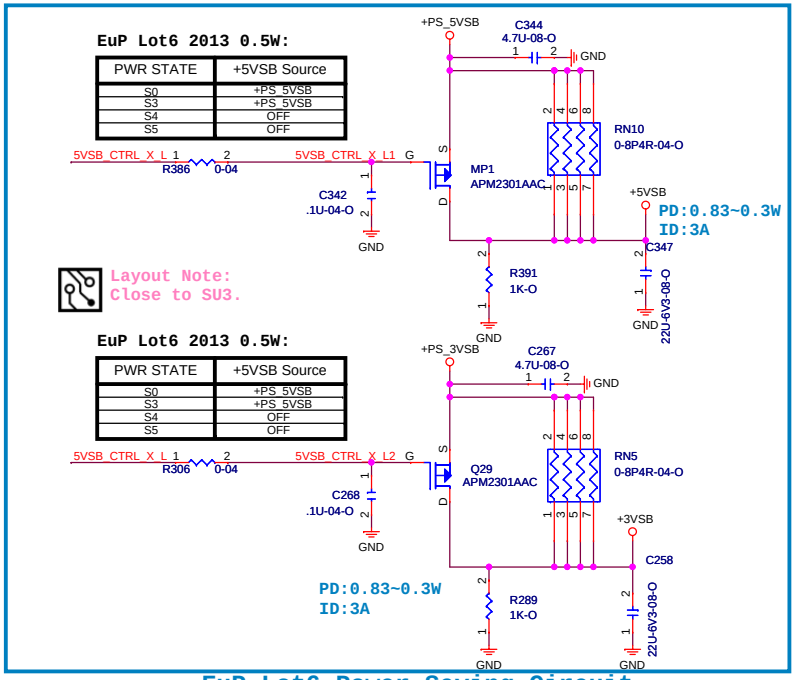
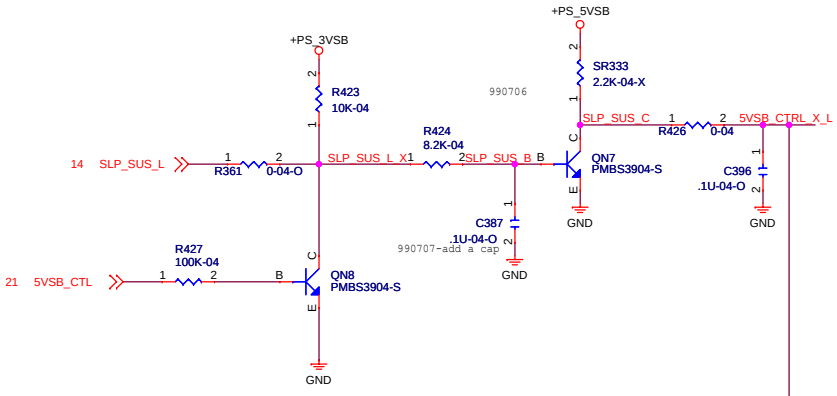
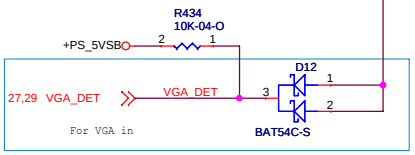
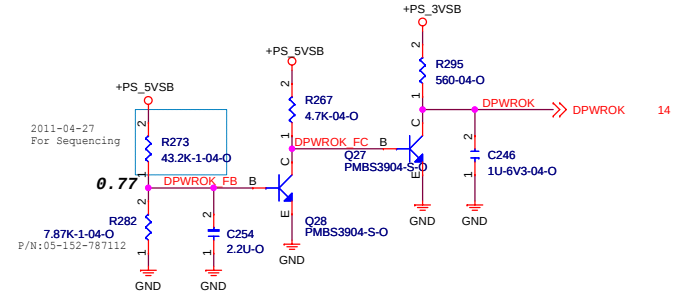


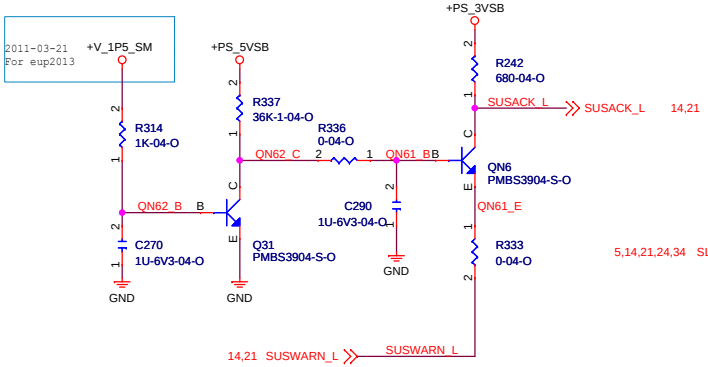


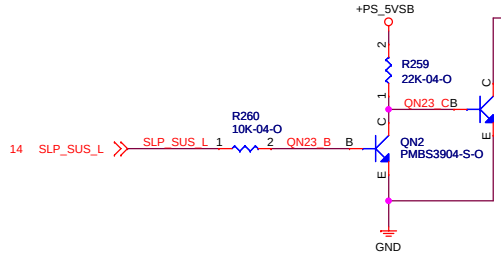


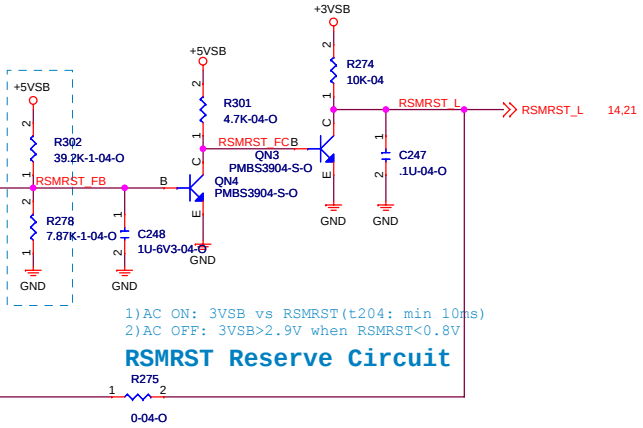
3VSB Non-EuP Lot6 Mode:

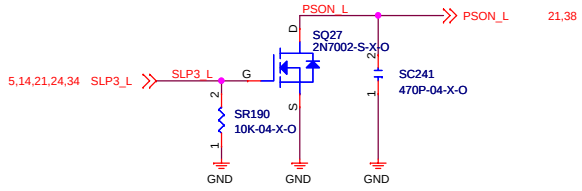
Power Name	Current
4 Slots	0.375 X4 = 1.5A
LAN	16m + 49m = 65mA
PCH	123mA
	50mA
EPW	16mA
SPI	mA
SIO	mA
Total Current	+ 1.754 A











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Title	DC/DC 3VDUAL/Deep Sleep	
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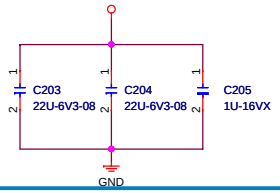
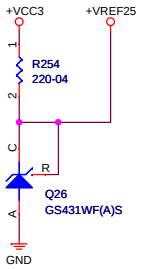
V1P05_ME

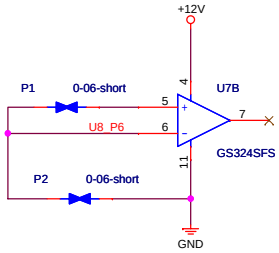
V1.05_ME connect to V1.05_PCH
1.05V
MAX 1.8A

+V_1P05_PCH

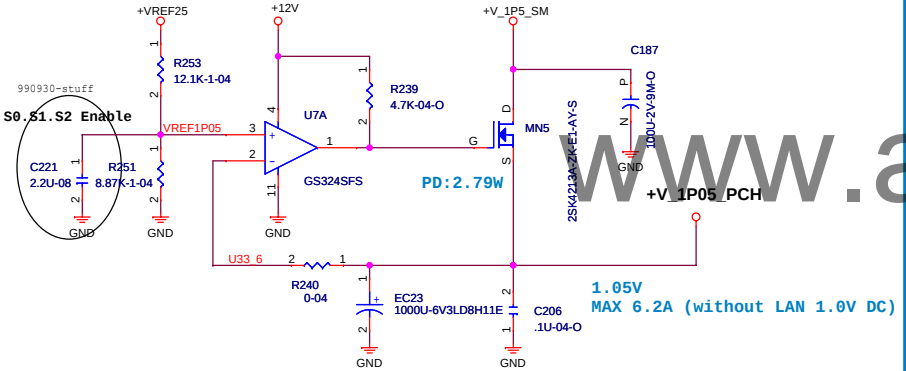


VREF25

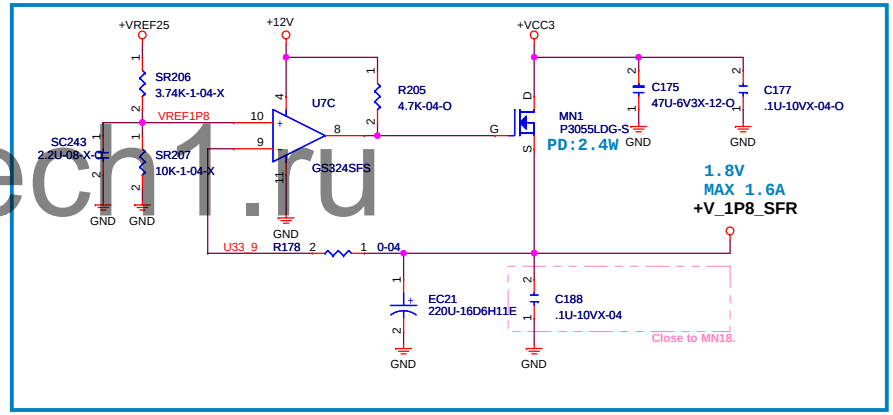




V1P05_PCH



V1P8_SFR(1.6A max)



Elitegroup Computer Systems

Title	DC/DC V1P05_PCH,ME/V1P8_SFR	
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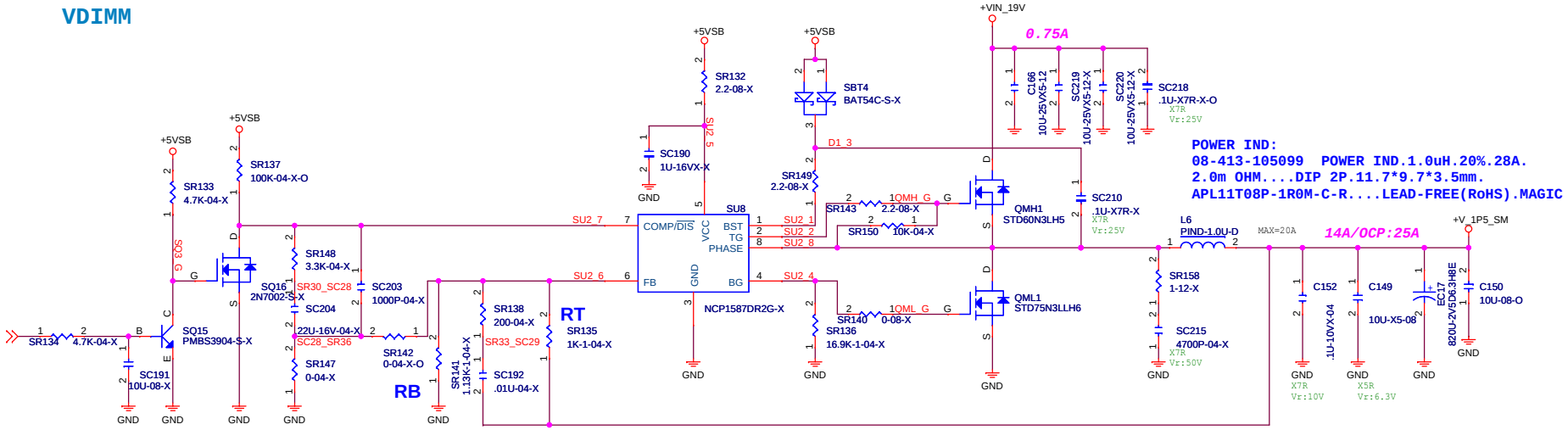
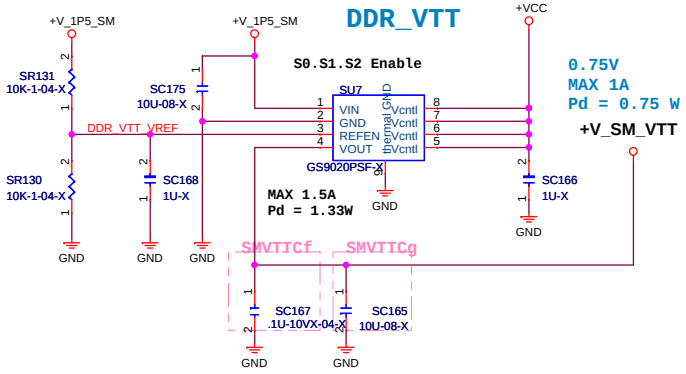
DDR3 POWER

VDIMM



Switching Output Voltage=0.8V*(1+RT/RB)

DDR_VTT



Layout Note:
SMVTTCf close to U39 Pin4.
SMVTTCg are between Channel A & B.
SMVTTCh are between Channel A & CPU.

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Title	DC/DC VDIMM/DDR_VTT/5VDUAL	
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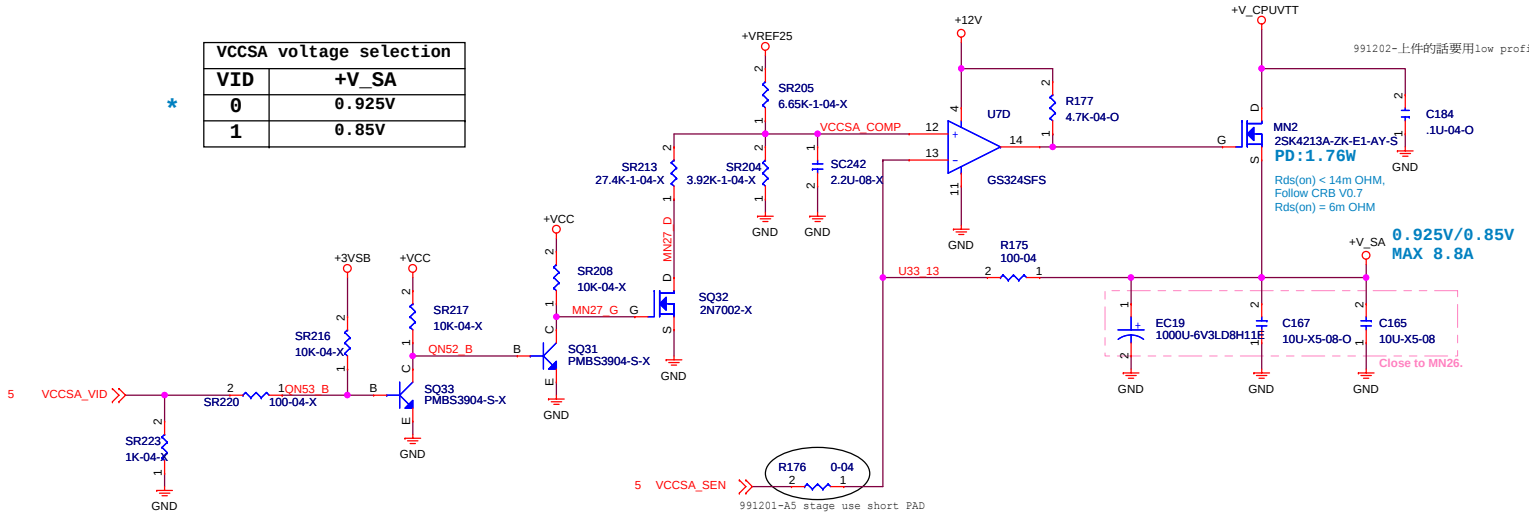
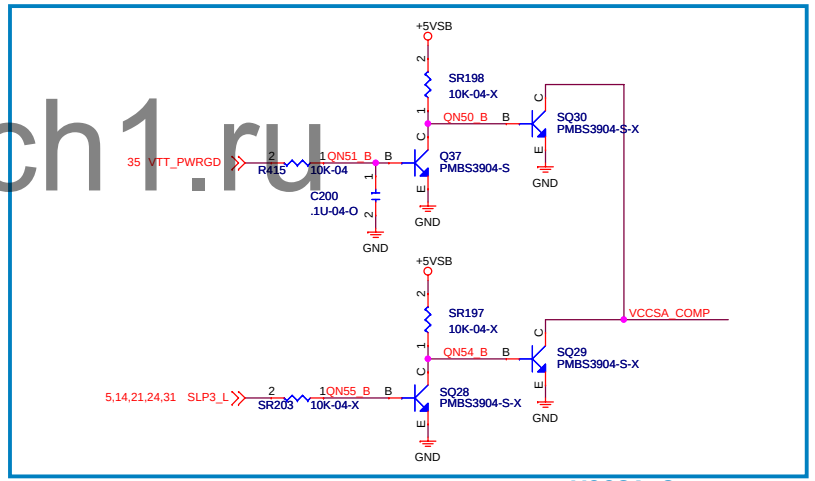
VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

*





VCCSA Sequence

Elitegroup Computer Systems

Title	DC/DC VCCSA, ATXPWR	
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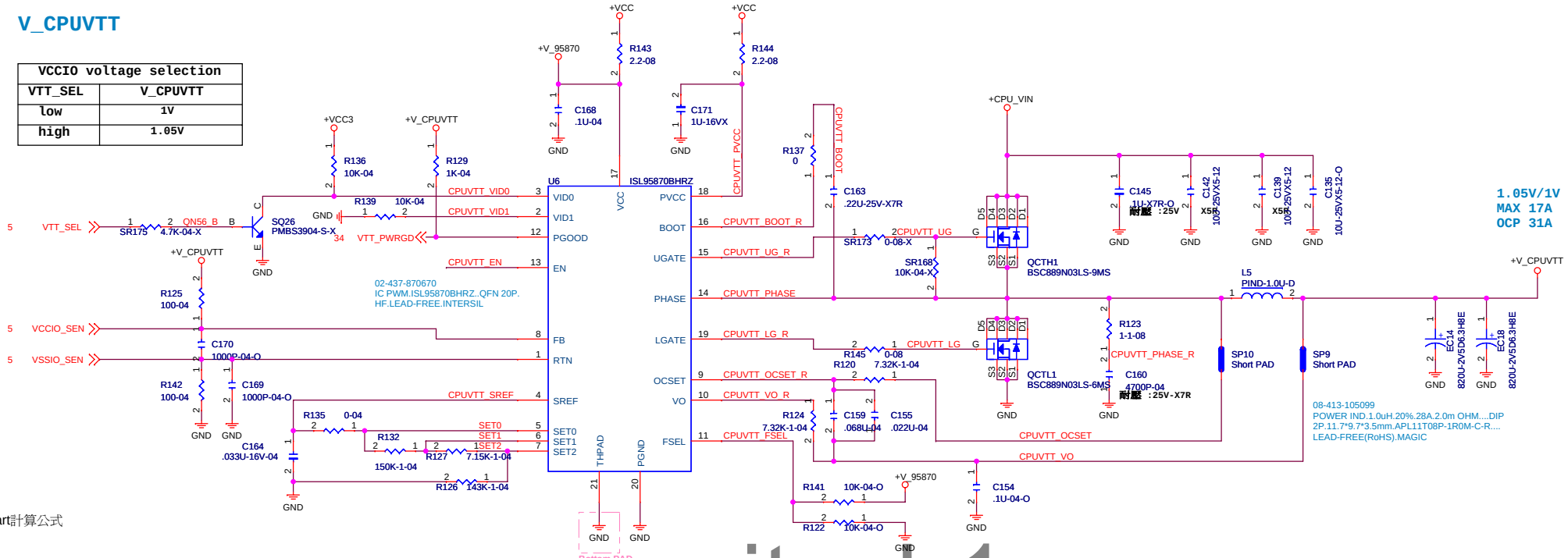
V_CPUVTT

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad \text{(EQ. 1)}$$

Vout計算公式

Where:

- I_{SS} is the soft-start current source at the 20µA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Frequency selection	
F(Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC

Note

1. Rocset = Iout*DCR/Iocset ; Iocset = 10uA
   If DCR = 2m ; Iout = 20A, Rocset = 20A*1m/10uA --> Rocset = 2K
2. Csen = L/Rocset*DCR
   If DCR = 2m ; L = 1U, Csen = 1U/2K*1m --> Csen = 0.5U

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT		
VID1	VID0	CLOSE	V_{SREF}	V_{OUT}
1	1	SW0	V_{SET1}	V_{OUT1}
1	0	SW1	V_{SET2}	V_{OUT2}
0	1	SW2	V_{SET3}	V_{OUT3}
0	0	SW3	V_{SET4}	V_{OUT4}

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

The ISL95870B V_{SET1} setpoint is written as Equation 21:

$$V_{SET1} = V_{REF} \quad \text{(EQ. 21)}$$

The ISL95870B V_{SET2} setpoint is written as Equation 22:

$$V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 22)}$$

The ISL95870B V_{SET3} setpoint is written as Equation 23:

$$V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right) \quad \text{(EQ. 23)}$$

The ISL95870B V_{SET4} setpoint is written as Equation 24:

$$V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right) \quad \text{(EQ. 24)}$$

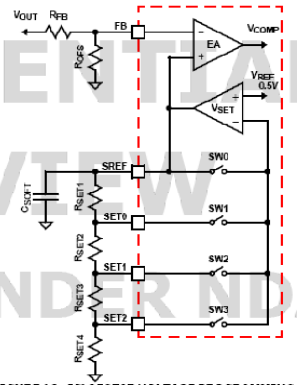
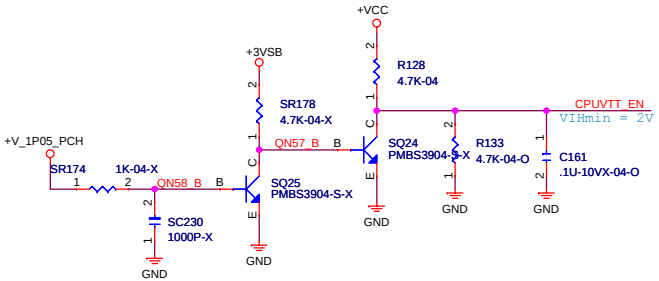


FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT



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Title	DC/DC V_CPUVTT	
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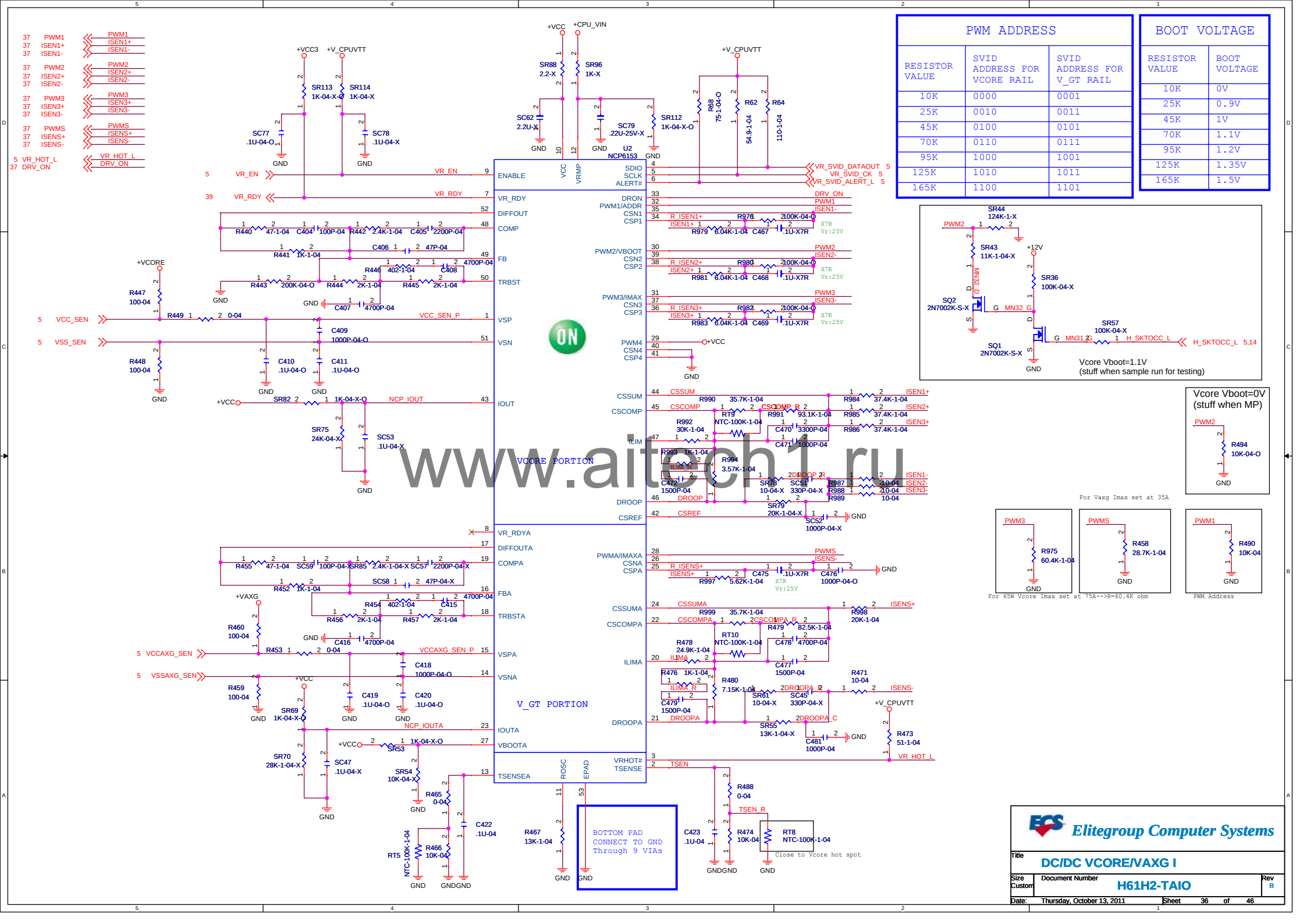

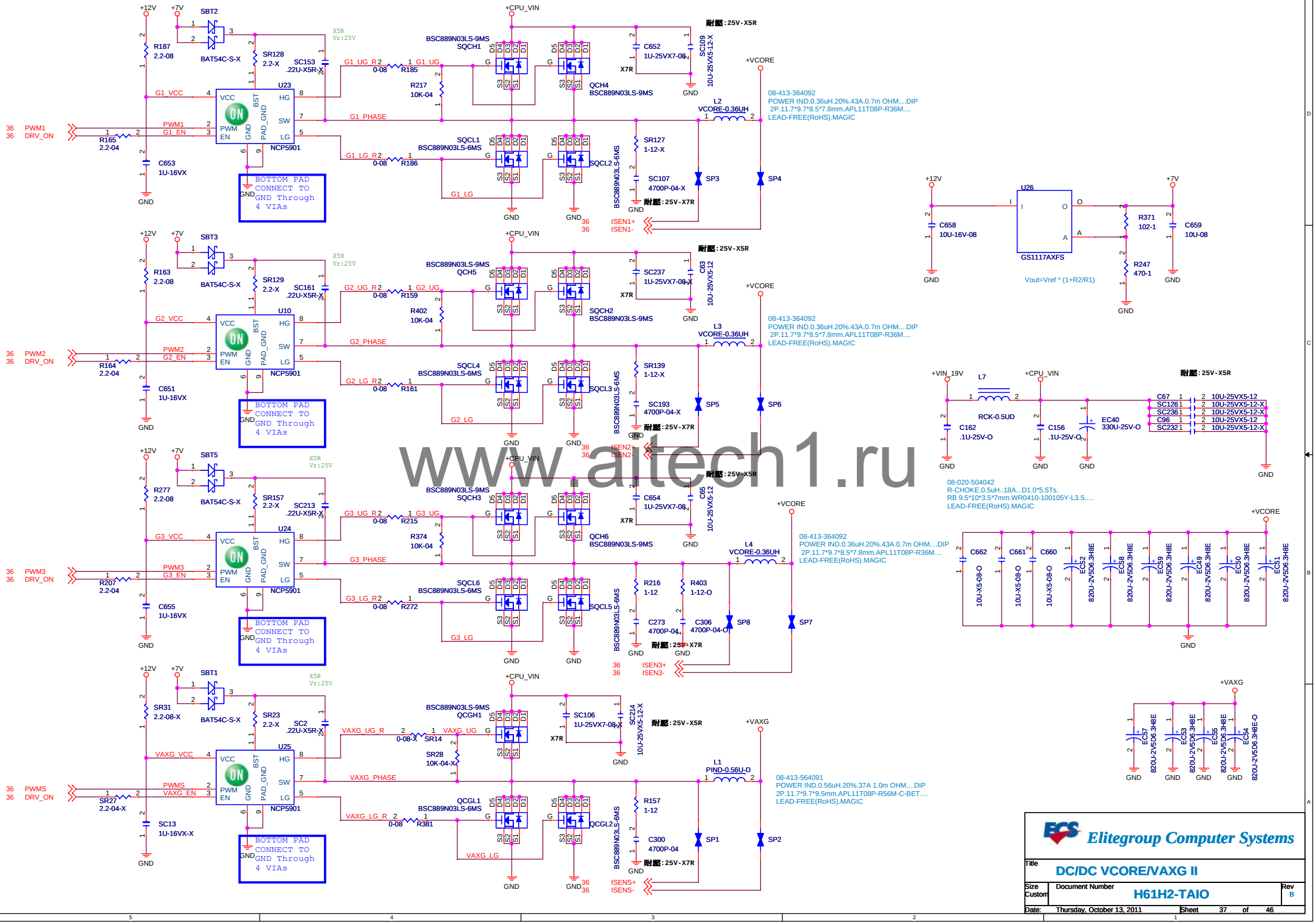

Elitegroup Computer Systems

Title	DC/DC VCORE/VAXG II	
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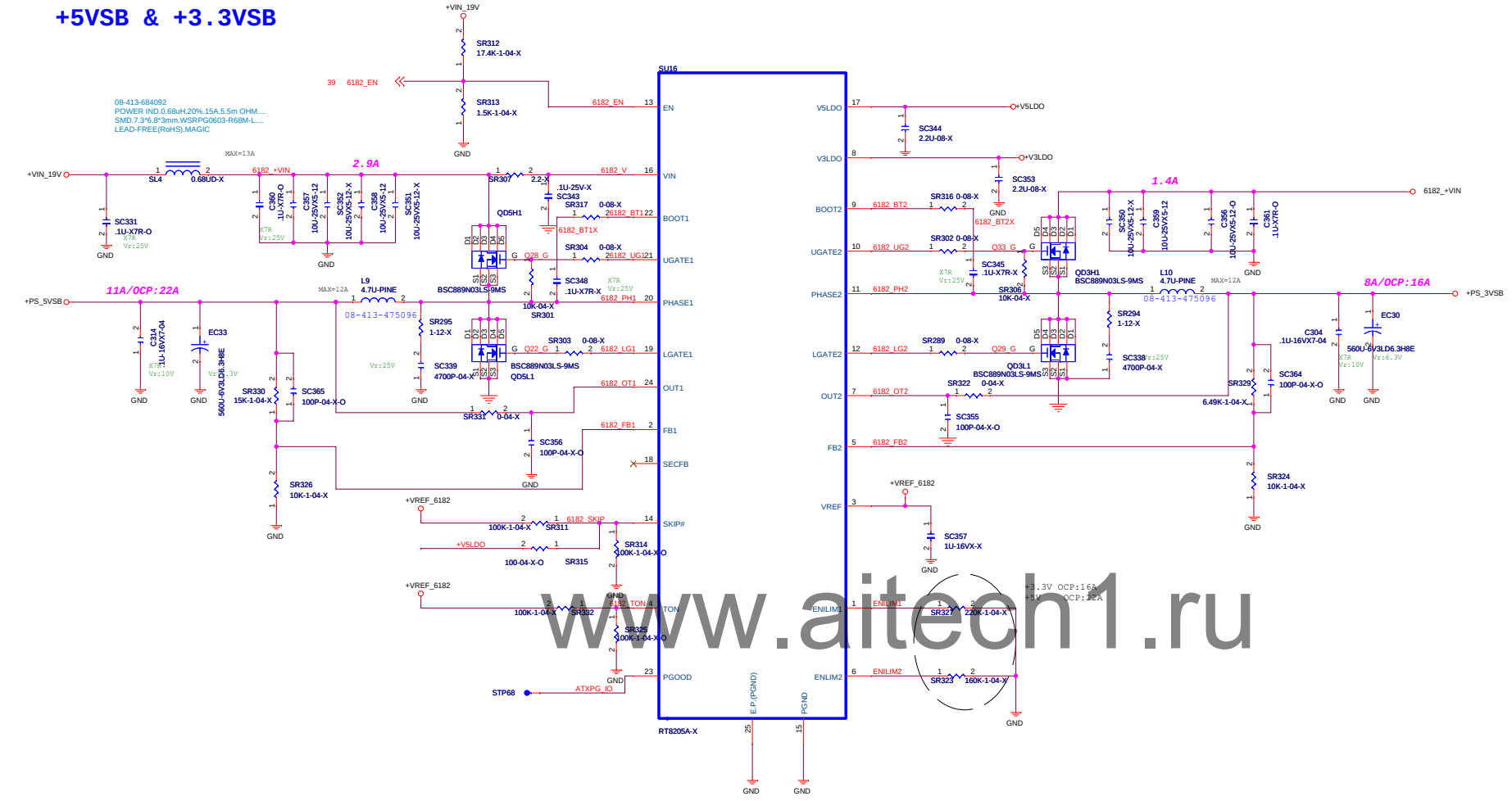
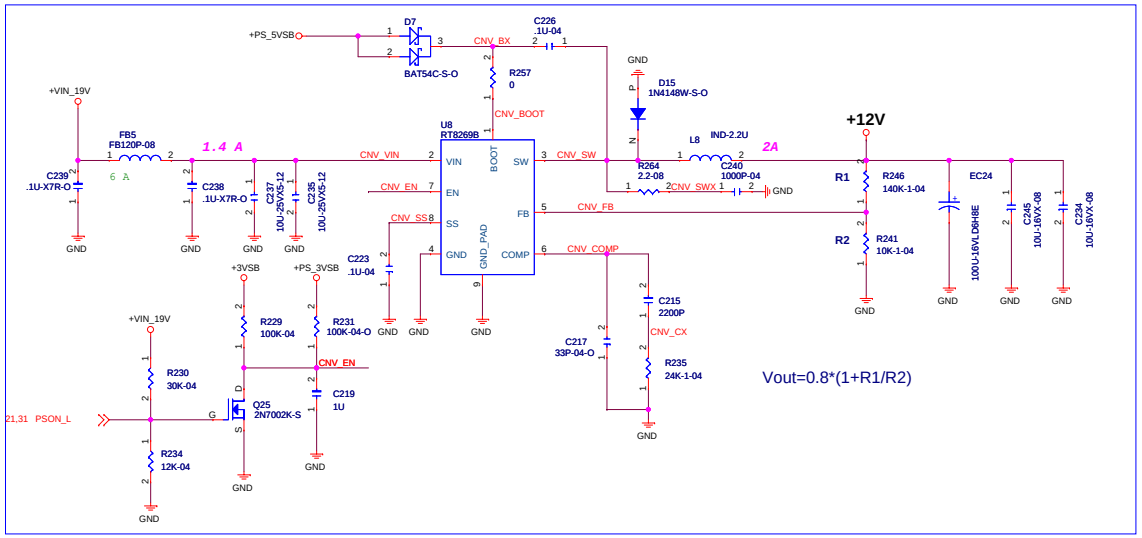
+5VSB & +3.3VSB





Elitegroup Computer Systems		
Title: 12/5VSB/3VSB		
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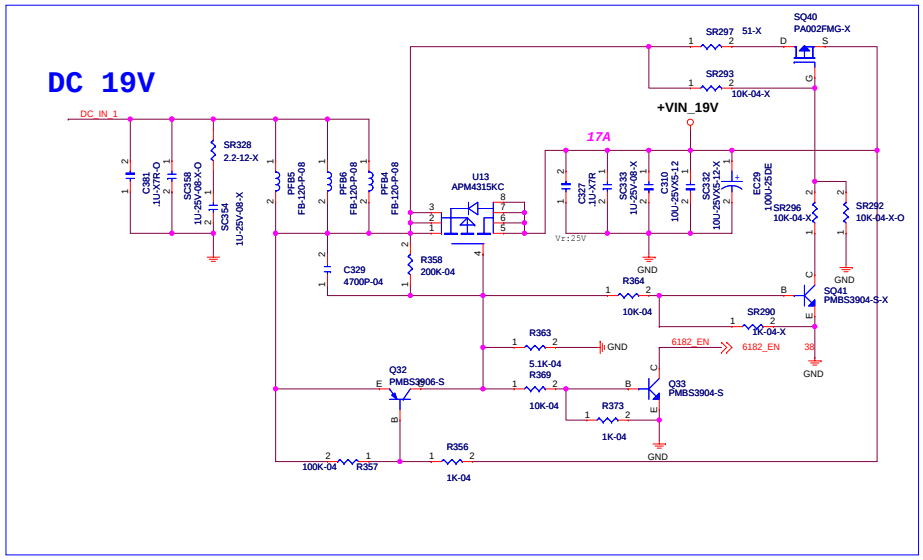
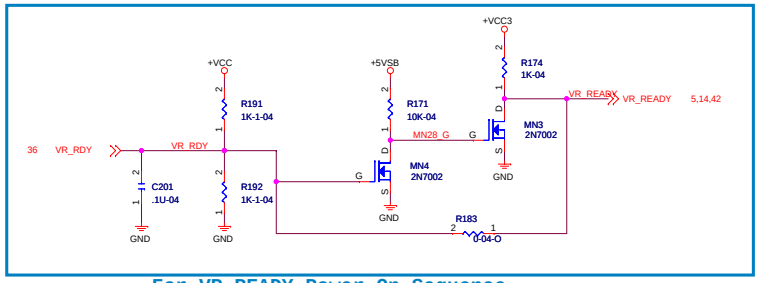
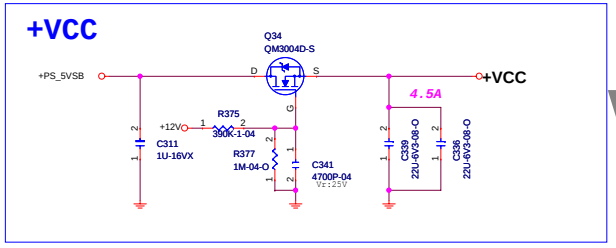
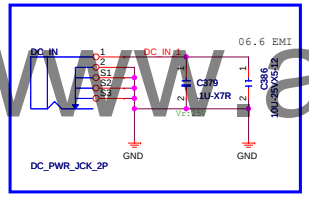
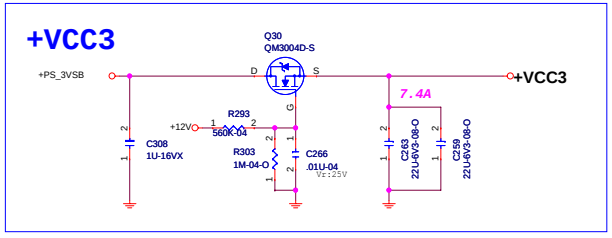




For VR_READY Power On Sequence







<OrgAddr1>	Elitegroup Computer Systems	
Title	DC/DC 19V/VCC/VCC3	
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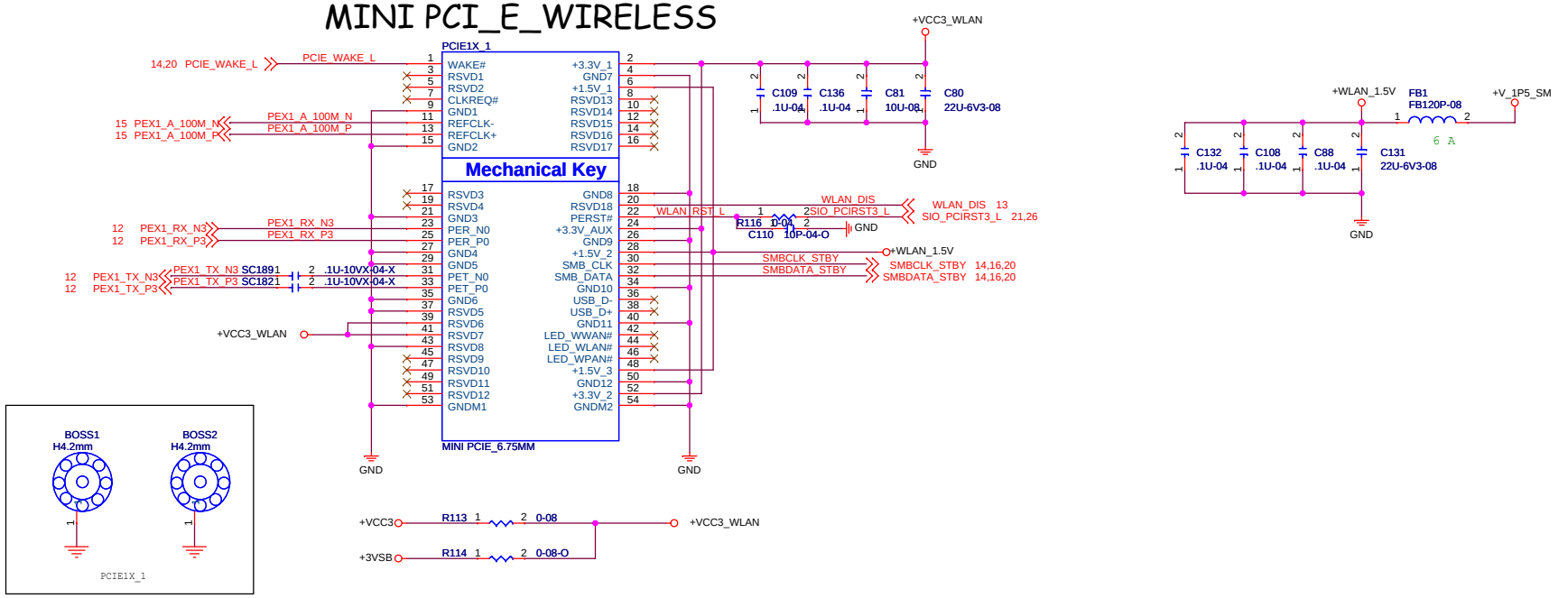
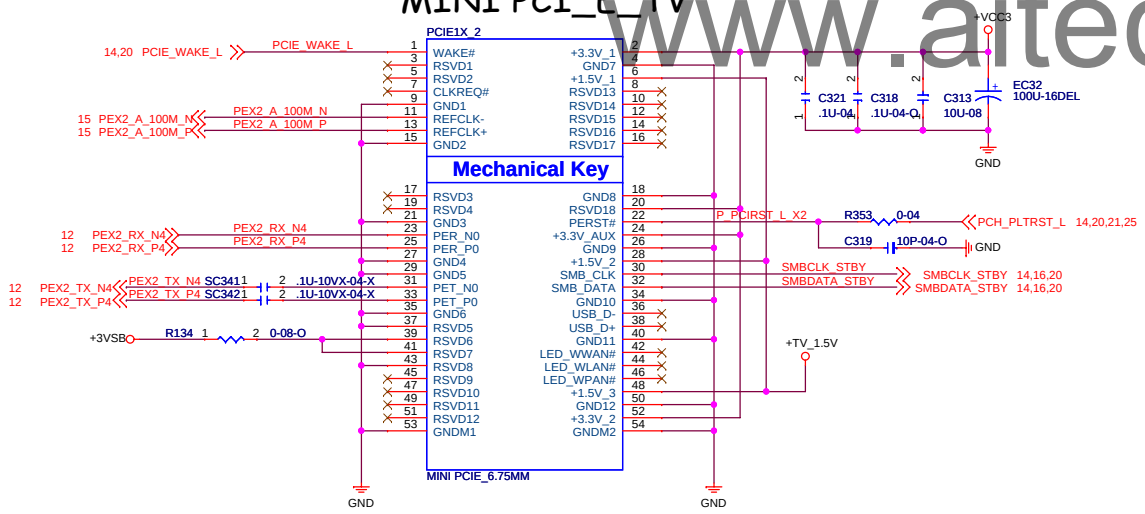
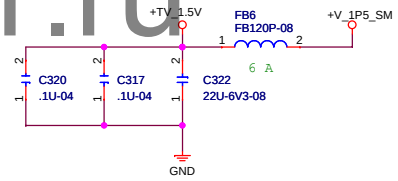
MINI PCI_E_WIRELESS



MINI PCI_E_TV





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Title	MINI PCIE(TV &WLAN)	
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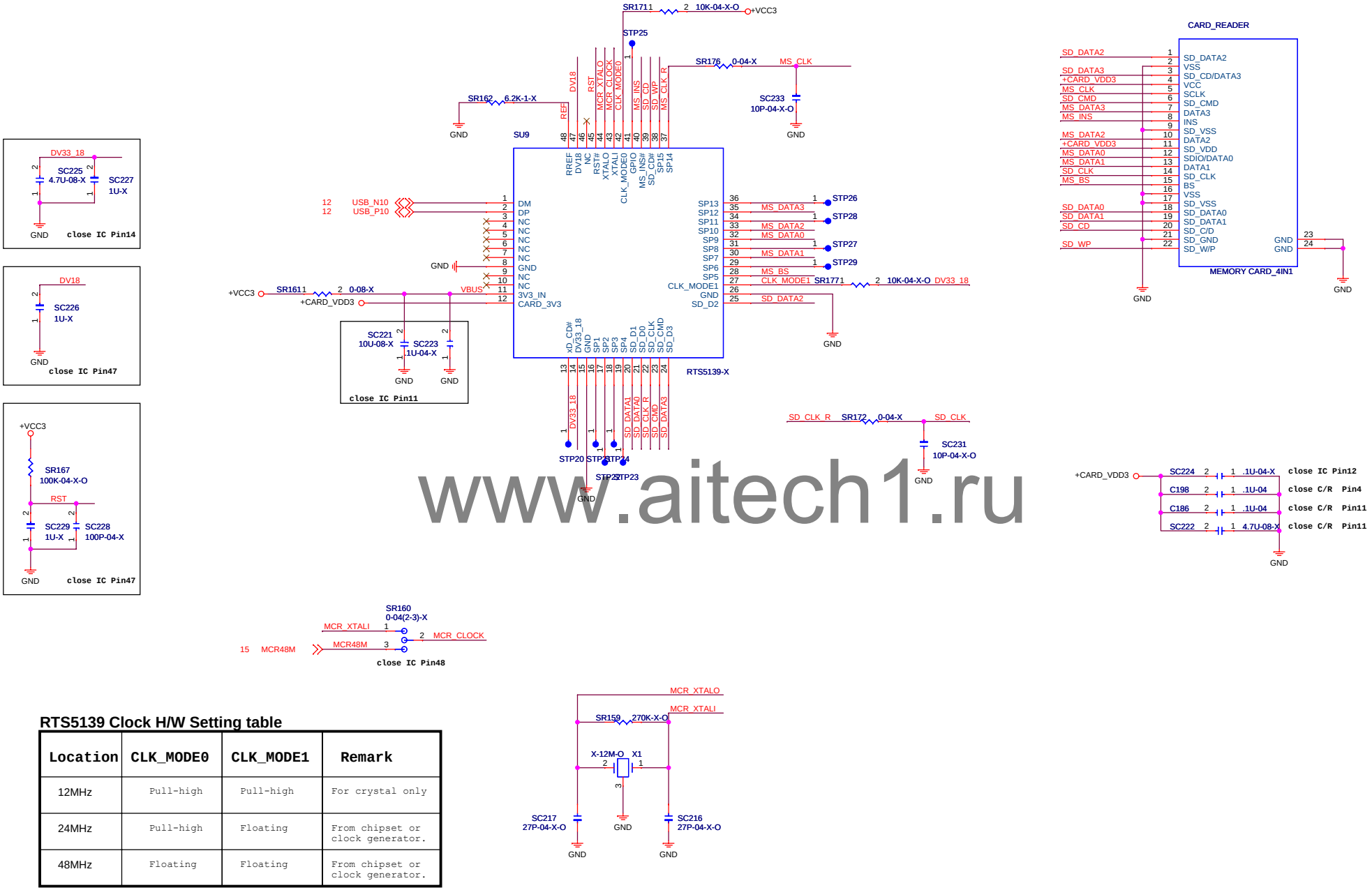

RTS5139 Clock H/W Setting table

Location	CLK_MODE0	CLK_MODE1	Remark
12MHz	Pull-high	Pull-high	For crystal only
24MHz	Pull-high	Floating	From chipset or clock generator.
48MHz	Floating	Floating	From chipset or clock generator.

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Title: RTS5139

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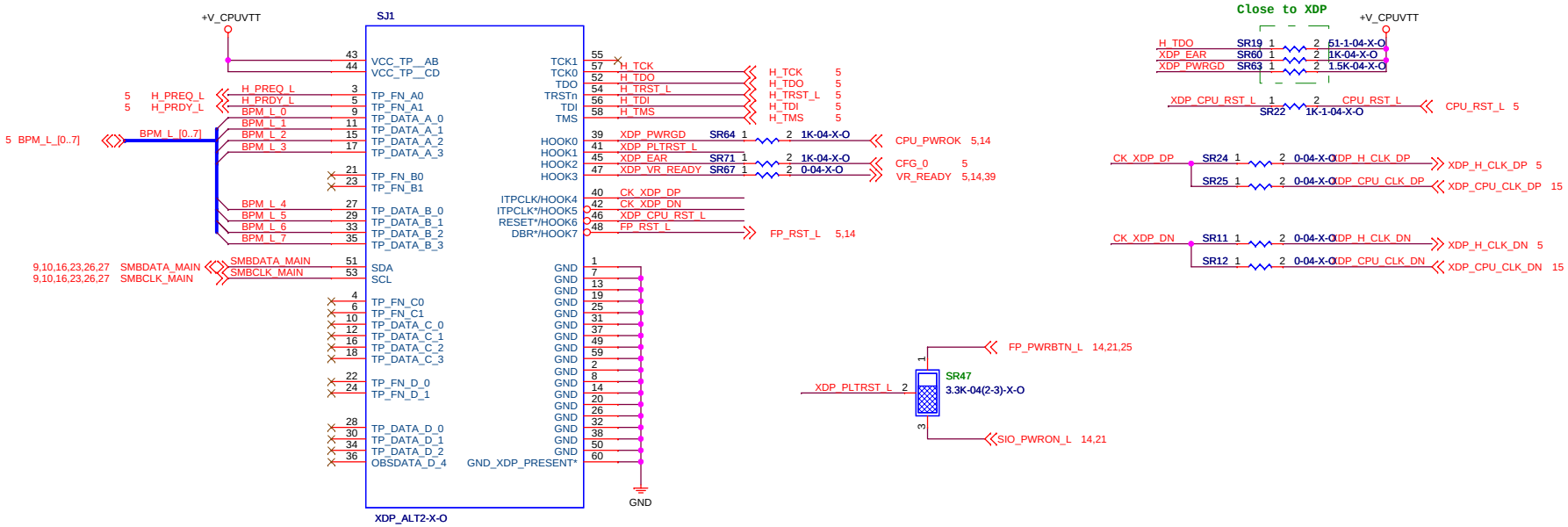

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Title: XDP

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PCH Strap Pin

Pin Name	Usage	Default Status
SPKR	No Reboot	20K internal pull-down，No Reboot Mode with TCO Disabled:
INIT3_3V#	Reserved	20K internal pull-up，intend for Firmware Hub.
GNT[3]#/GPIO[55]	Disable Top-Block Swap	20K internal pull-up，“topblock swap” mode Disable
INTVRMEN	Enable Integrated 1.05V VRM	Need External Pull-up，Integrated 1.05V VRM Enable
GNT1# /GPIO51	Boot BIOS Strap bit [1] BBS[1]	20K internal pull-up，The default flash selection is the SPI flash.All
SATA1GP / GPIO19	Boot BIOS Strap bit[0] BBS[0]	20K internal pull-up，The default flash selection is the SPI flash.All
HDA_SDO	Flash Descriptor Security Override/ ME	Internal pull-down. The security measures defined in the Flash Descriptor will be in effect(default)
DF_TVS	Enable DMI termination voltage	This signal has a weak internal pull-down.
GPIO28	Eable On-Die PLL Voltage Regulator	The On-Die PLL voltage regulator is enabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select 1.8V	20K internal pull-down.On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low.
GPIO15	Enable TLS Confidentiality	Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality.

Boot Device Select:

	BOOT DEVICE	GNT1_L	GPIO19
	LPC	0	0
	PCI	1	0
*	SPI	1	1

Disable ME Jumper:

	MODE	CLR_RTC
*	Normal	1-2
	Disable ME	2-3

HDA_SDOUT_R (internal PD)

CLEAR CMOS Jumper:

	MODE	CLR_CMOS
*	NORMAL	1-2
	CLEAR CMOS	2-3

Power-On Strapping

	Symbol	Value	Description
JP1 Pin-23	DSW_EUP_SEL	1 *	EUP(default)
		0	DSW
JP2 Pin-57	WDT_EN	1	Disable WDT to reset PWROK(default)
		0 *	Enable WDT to reset PWROK
JP3 Pin-59	FAN_CTL_SEL	1 *	EC Index 6Bh/73h default = 80h
		0	EC Index 6Bh/73h default = 00h
JP4 Pin-61	K8PWR_EN	1 *	Disable K8 Power Sequence(default)
		0	Enable K8 Power Sequence

CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

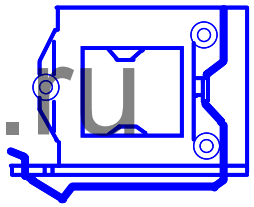
	PCIE CONFIG	SEL0	SEL1
*	1 X 16	1	1
	2 X 8	0	1

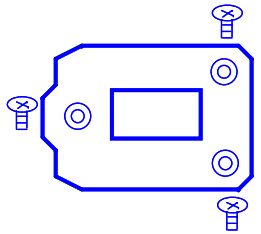
CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

11-018-115122
SOCKET.CPU..LGA 1155P SMD..15u...BLACK.ACA-ZIF-096-P01...HF.LEAD-FREE.LOTES

20-800-004611
SUBASSY.STEEL....LGA 1156P.....W/BACK PLATE.ACA-ZIF-082-K01....LEAD-FREE(RoHS).LOTES

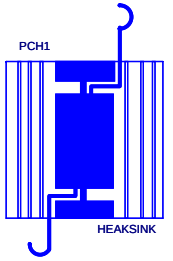
CPU2
CPU_SUBASSY_STEEL



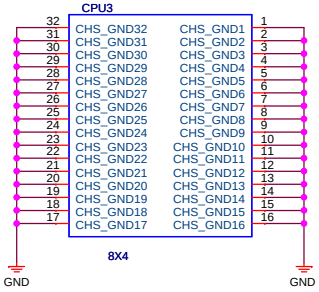


PCH heatsink P/N:
20-120-014520
20-120-014511
20-120-014512

PCH1

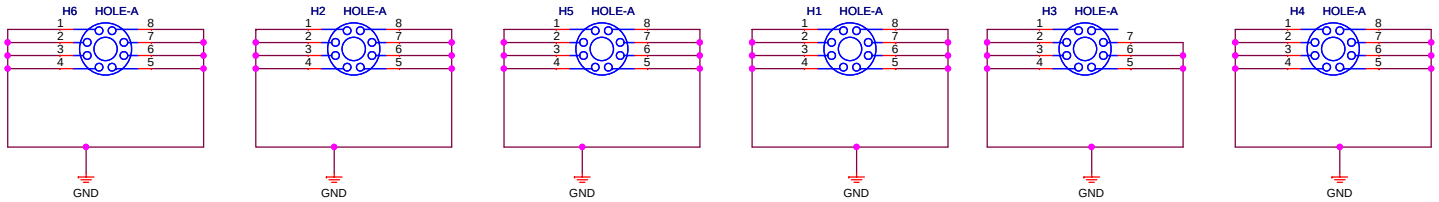


CPU3



Y1_JP

For 104



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Title: 104 & STRAPPING

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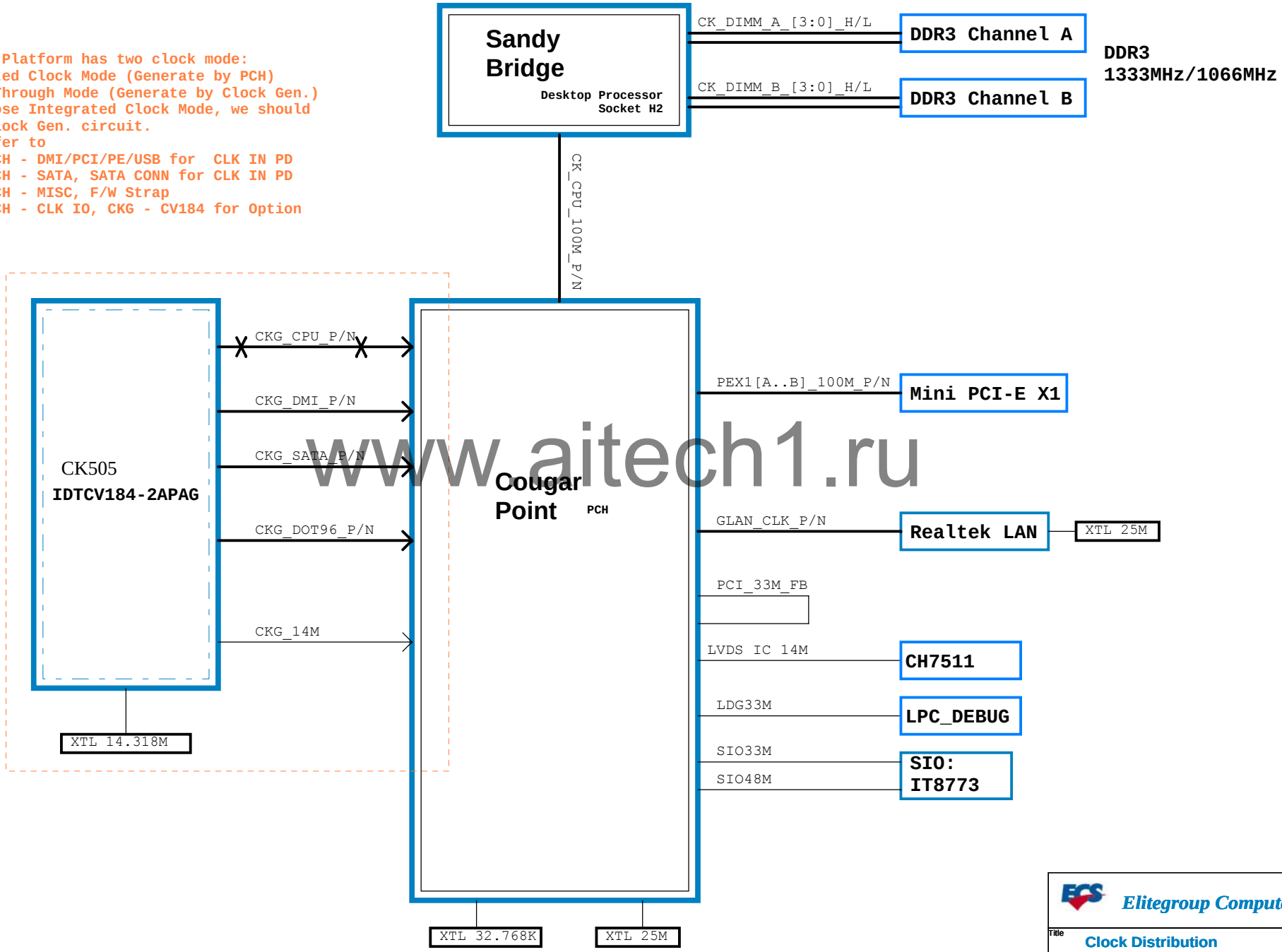
NOTE:
Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
Please refer to
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
Page.13 PCH - SATA, SATA CONN for CLK IN PD
Page.14 PCH - MISC, F/W Strap
Page.15 PCH - CLK IO, CKG - CV184 for Option



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Title: Clock Distribution

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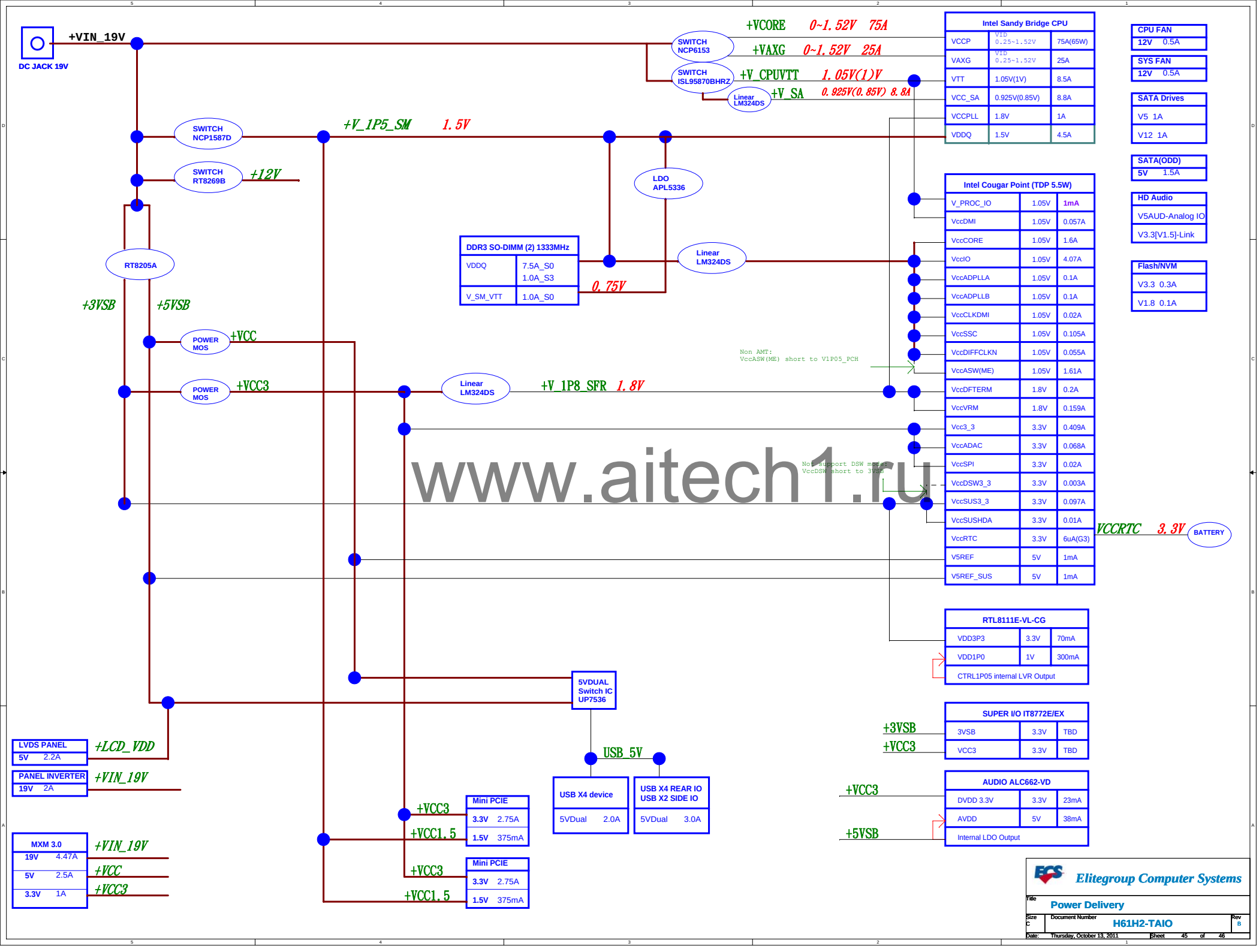

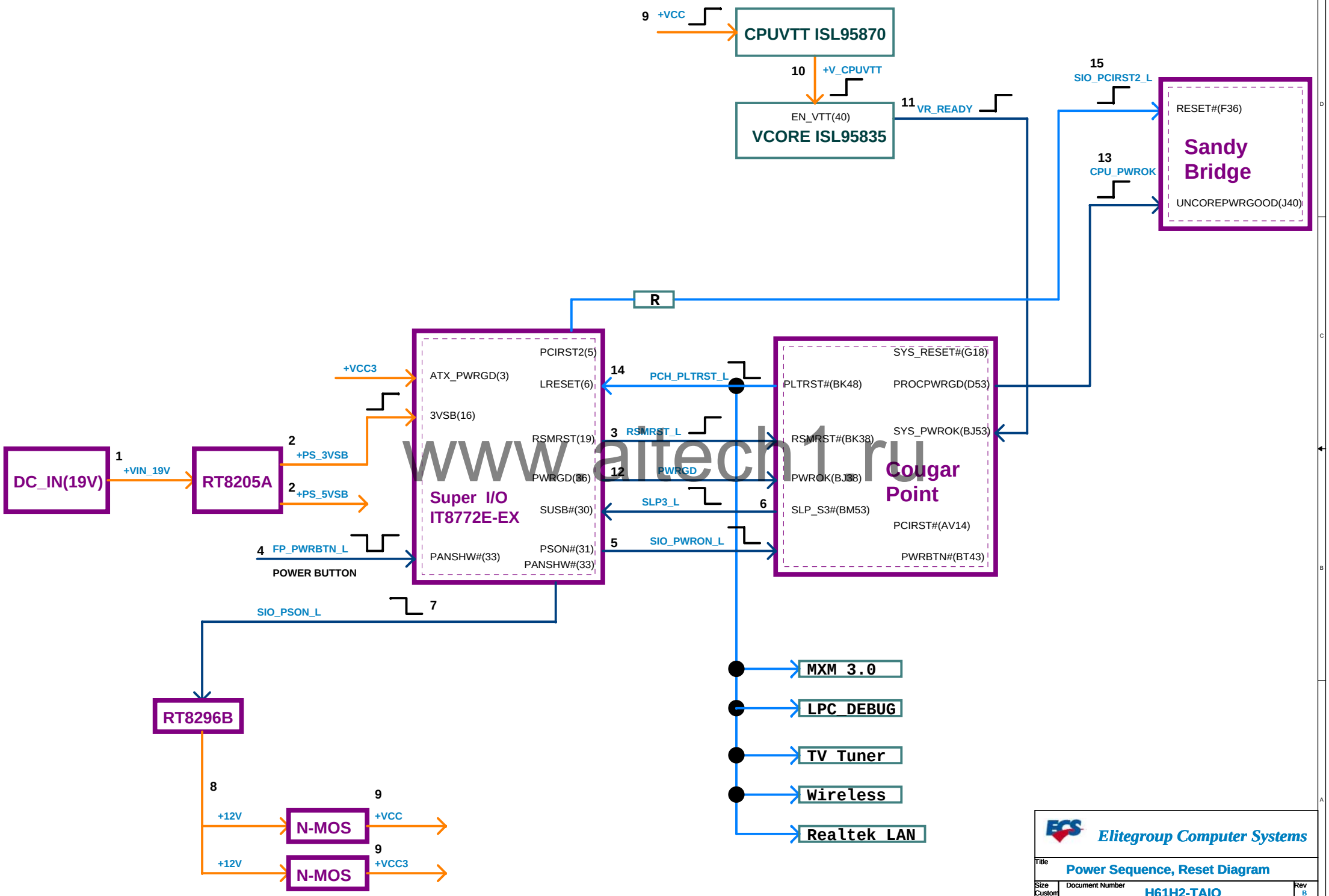

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Title: Power Sequence, Reset Diagram

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